PSERC

Digital Protection System Using Optical Instrument Transformers and Digital Relays Interconnected by an IEC 61850-9-2 Digital Process Bus

Final Project Report

Power Systems Engineering Research Center

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Power Systems Engineering Research Center

Digital Protection System Using Optical Instrument Transformers and Digital Relays Interconnected by an IEC 61850-9-2 Digital Process Bus

Final Report

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Power Systems Engineering Research Center

This is a project report from the Power Systems Engineering Research Center (PSERC). PSERC is a multi-university center conducting research on challenges facing a restructuring electric power industry and educating the next generation of power engineers. More information about PSERC can be found at the Center's website: http://www.pserc.org.

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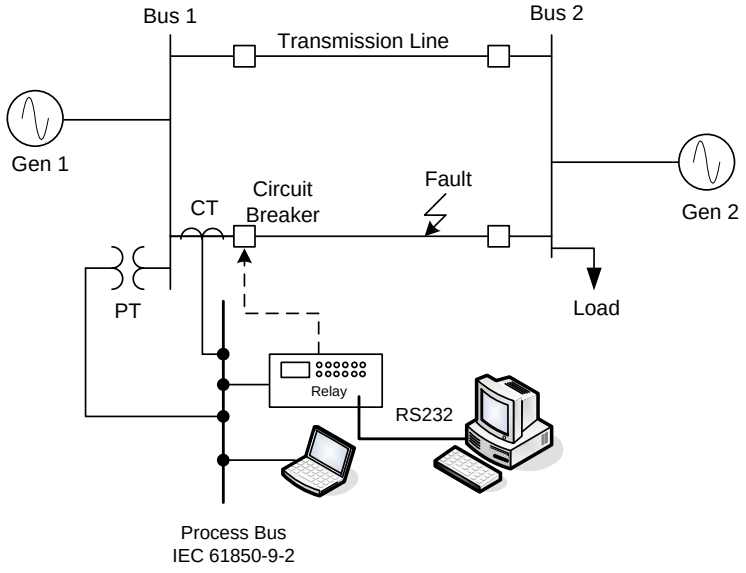
Executive Summary

All-digital systems for measurement, protection and control with components from different manufacturers are increasingly being deployed in electric power substations. As this occurs, a critically important task becomes the verification that required performance and expected design criteria are satisfied for any specific system configuration and inter-device communications standard. Of particular focus in this research is the development of a methodology for testing device interoperability under the International Electrotechnical Commission (IEC) Standard 61850-9-2 on communication interfaces in substations. The methodology includes evaluation criteria, which is important because current test and evaluation activities defined by professional groups, such as the Utility Communication Architecture (UCA) International Users Group, do not define criteria for evaluation of integrated systems comprising digital transducers, merging units, digital switches and digital relays with low power inputs.

A digital protection system typically consists of optical instrument transformers, a digital communication bus, and a digital relay for operating a circuit breaker when needed as illustrated below. An optical instrument transformer measures the line voltage and current values, and sends digitized measurement data to a digital relay through a digital communication process bus. A digital relay processes the data using algorithms such as for over-current protection and for distance protection. When a fault is detected, the relay trips a circuit breaker and triggers an alarm signal that could be communicated, for example, to a display terminal via a RS232 line as shown below.



The selected methodology was designed to meet two objectives: testing under a variety of conditions that allow sensitivity analysis for statistical evaluations and testing under a real-life operating environment. To reach those objectives, two testing approaches were used: a) laboratory testing using a digital simulator producing low-level signals feeding the instrument transformer transducers, and b) high-power laboratory testing using high-level signals feeding a real-life instrument transformer transducer. The first step was

accomplished by a Texas Engineering Experiement Station research team led by Dr. Kezunovic and the second by the research team at Arizona State University led by Dr. Karady. Both activities tested prototype digital products from participating vendors.

Part I: Low-Level Testing

The principal tasks of the low-level testing was the analysis of all digital measurement and protection system operation using a digital simulator test bench to compare the compatibility and interoperability of products provided by different manufactures. Compatibility tests verify that different parts of the all-digital system supplied by a given vendor can operate together. Interoperability tests verify that the all-digital system components can be interchanged with products from different vendors. Tests were conducted with simulation software with models of all the evaluated equipment. Compatibility indices were defined and calculated by analyzing output signals of the IEDs. Simulated scenarios were selected to create power system conditions in which the correct operation of the protection system was critical. The protection function selected for evaluation was overcurrent protection which is expected to operate (issuing a trip command) for faults in the forward zone of protection and not operate for faults in the backward zone. The overcurrent relay functions tested were: a) three-phase directional instantaneous overcurrent protection as primary protection; b) three-phase time overcurrent protection as backup protection; and c) residual time overcurrent protection.

Results obtained using the testing methodology allowed determination of the performance level and compatibility between system elements (i.e., products), how the measured performance of elements compared to each other, what elements of the system contributed to problematic system performance and under what conditions problematic performance occurred. Results were obviously dependent upon the equipment and system configuration. The following actual results illustrate what might be found using the developed testing methodology:

- Performance of the system is excellent for the directional overcurrent protection function.
- The system's operating time for any given fault follows the operating time-current characteristic with almost a negligible level of dispersion from the mean trip time (around 2 ms).
- Overall protection system performance is not affected by interchange of Ethernet switches. Differences in performance indices were negligible given the nominal traffic load on the process bus and the low level of electromagnetic interference in the laboratory. Ethernet switch interoperability should be further tested in a harsh environment with a high traffic load.
- Interchanging sensors and merging units did not make an appreciable difference in overcurrent performance indices. Testing based on the same input signals and relay settings showed that there was no significant difference in protection system performance.
- Interoperability indices values showed that the equipment in tested protection systems were compatible and could be interchanged without significant effect on

protection system performance. Sensors and merging units interchanged during these tests had very similar performance characteristics.

Part II: High-Power Testing

A laboratory test facility was configured to test an all-digital protection system using high voltage and high current that simulate a power line fault. Due to the difficulty of generating high voltage and high current at the same time under laboratory conditions, a laboratory configuration was constructed with a high current generator and a high voltage generator. Both generators were supplied by the local low voltage network.

In the high current generator three, ring-type current transformers generated the fault current when an electronic switch energized the five ampere secondary winding of the current transformers. The short circuit could be initiated at any time between zero and 180 degrees on the source voltage wave. A similar system produced the pre-fault load. The discharge of a capacitor bank provided the variable DC offset.

In the voltage generator, the pre-fault input to the high voltage transformer was controlled by a regulating transformer. The post-fault voltage magnitude was controlled by an adjustable voltage-dip generator. The timing of the voltage change was controlled by an electronic switch that was synchronized to the fault initiation.

High fault current (few thousand amperes and DC offset current) and high fault voltage (10kV to 69kV) were generated simultaneously and supplied to the equipment under test. Both optical and traditional instrument transformers can be connected to the test system at the same time and the output of the transformers can be connected to digital and analog relays to observe the responses in simulated fault conditions.

This test facility was used to test an all-digital protection system that included an optical current transformer with a digital output signal. The digital relay was tested in over-current mode. The overall conclusion for the particular equipment and configuration tested was that the all digital over-current protection operated well and the all digital system would be suitable to protect electric power systems where over-current protection is needed. However, the testing showed that there was a significant mismatch between the current values measured by the digital relay and by the optical current transformer; this mismatch suggested a need for corrections to the manufacturers' software.

An all-digital protection system was tested in inverse over-current mode. The system operated well and cleared the faults with proper delay. The relay measured the current dependent time delay accurately; however, the time delay computed using the manufacturer's equation was different than what actually occurred, suggesting the need for a review of the software. The test results also showed that the load current and short duration impulse currents do not produce misoperation. Also, the DC offset current does not adversely affect the tripping time.

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1.0 Introduction

This report presents results of tasks, defined in the statement of work for project titled "Digital Protection System Using Optical Instrument Transformers and Digital Relays Interconnected by an IEC 61850-9-2 Digital Process Bus." The tasks are: Analysis of an all digital measurement and protection system operation using a digital simulator test bench and overall comparison of the compatibility of systems provided by different manufactures. This report presents evaluation criteria, methodology, and test implementation. Tests were implemented through extensive simulation software. Simulation environment encompasses models of all the equipment involved in the evaluation.

2.0 Evaluation Criteria

2.1 Introduction

Evaluation of the all-digital system performance is necessary in order to recognize all possible conditions when protection system may miss-operate, or operate with unacceptable performance (reduced selectivity, increased operating time, etc). Identifying these abnormal situations is important for two reasons: a) recognizing possible conditions for incorrect operation, b) proving that the novel implementation will not translate in degrading protection system performance. This chapter defines a set of criteria that can be used for numerical evaluation of the all-digital protection system performance. Instrument transformers (also referred to as transducers) and protection relays (IED) are elements of the protection system. Criteria will be defined separately for the mentioned elements.

2.2 Shortcomings of the Existing Performance Evaluation Criteria

Criteria for performance evaluation of the protection system is not a new topic and has been investigated in earlier research efforts [1], [2], [3]. Although the proposed criteria have proven to be effective to evaluate the performance of conventional protection system, their scope is limited. The compatibility evaluation is a necessity introduced by the implementation of a digital protection system, hence the criteria need to be extended to be applicable for all-digital systems.

There are two known criteria to evaluate the performance of protection systems:

1. Criteria presented in [4] define protective relay performance as:
   a) Correct operation; b) Incorrect operation; and c) No conclusion
2. Criteria presented in [2] evaluate protective relay performance based on:
   a) The measuring algorithm; and b) The decision making algorithm

Even though both performance characterizations can be useful, they suffer from certain shortcomings when applied to the all-digital system:

- In the case of the first set of criteria presented above, classes are too broad and they do not provide a complete assessment of the overall performance of the protective relay. There are no means to differentiate performance of two different relays with respect to specific performance characteristics such as: operating time, correct fault type identification, fault locator accuracy, etc.
- In the case of the second set of criteria, they do provide to some extent means for a complete assessment of protection performance. However, the evaluation of the measuring algorithm only fits conventional relays. Relays compliant with digital process bus are not required to have a measuring algorithm which will trace the analog signals since the inputs are inherently digital.

The above shortcomings make these criteria insufficient when evaluating performance of a process bus based protection system. In order to evaluate the performance of this novel system, a new methodology needs to be defined.

2.3 Referent Models

In order to evaluate how the performance of the all-digital protection system measures up to the performance of the conventional protection, the concept of referent transducer system and protective relay is introduced. A comparison of performance and compatibility index values is necessary. A difference in the values of performance and compatibility indices between:

1. Referent protective relay exposed to signals supplied by a referent instrument transformer.
2. A process bus compliant protective relay exposed to signals supplied by novel electronic transducers serves as an indicator of the overall performance of a particular protection system (with specific electronic transducer and protective relay) when compared to the performance of the referent protection system.

The referent instrument transformer can be regarded as an ideal one that delivers exact signal replicas from the primary side. Even though this can not be achieved with actual instrument transformer designs, for practical purposes, this referent instrument transformer can be any transformer with an accurate, known and proven performance in field application. The referent protective relay is a software simulation model that accurately represents the behavior of a given protective relay. Several protective relay models with different operating principles such as overcurrent and impedance have been realized [5] [6].

2.4 Performance Indices

Performance evaluation aims at verifying the behavior of the protection system, accuracy and operating times under various power network conditions. Two sets of performance indices will be presented in this thesis: **relative** performance indices and **absolute** performance indices. Relative indices are dependent on a comparison between the protection system under study and a referent protection system. On the other hand, absolute indices are calculated by considering only the behavior of the protection system under study.

2.4.1 Relative indices

A number of performance indices for evaluation, design and setting optimization of measuring algorithms, operating principles, complete relays and protective systems are defined in details in [2]. This report will adapt some of the performance indices than can meet the needs of the all-digital protection system. The evaluation methodology is described in Fig. 1. The following definitions summarize the relative performance indices used in this report:

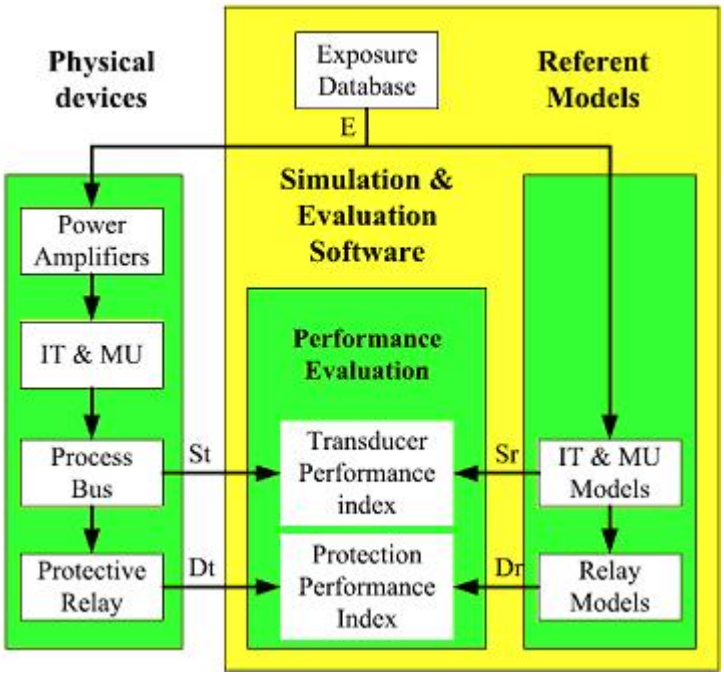

Figure 1. Performance indices calculation

Definition 1*: A single exposure E is a disturbance which triggers a protection system P to perform certain operations or other signals if called upon [2]. The exposures database EB is a database of exposures collected from the actual system or using simulators. Signal* S^t, S^r *denote the digital output of the tested and referent transducer system respectively. Decision* D^t, D^r *denote the decision of the tested and referent protection system respectively.*

Definition 2*: The performance index of transducer T when fed by exposure E is denoted by* TPI_T^E, $E=\{e_1,e_2,e_3,...,e_n\}$ *. The average performance index of transducer T is defined as:*

$$TPI_T = \frac{1}{N} \sum_{E \in EB} TPI_T^E \qquad (1)$$

where N is the number of exposures in the database.

There are two primary types of transducer performance indices calculation methods, namely the time domain method and frequency domain method respectively. For the time domain:

$$TPI_T^E = \sqrt{\sum_{i=1}^{n} (S_i^t - S_i^r)^2 / \sum_{i=1}^{n} (S_i^r)^2} \qquad (2)$$

For the frequency domain:

$$TPI_T^E = \sqrt{\sum_{j=1}^{m} (F_j^t - F_j^r)^2 / \sum_{j=1}^{m} (F_j^r)^2} \quad (3)$$

where F_j^t, F_j^r stand for the FFT coefficients of S_i^t, S_i^r respectively.

Definition 3: *The performance index of protection system P when fed by exposure E is denoted by* PPI_P^E. *The average performance index of protection system P is defined as:*

$$PPI_P = \frac{1}{N} \sum_{E \in EB} PPI_P^E \quad (4)$$

where N is the number of exposures in the database.

There are two types of protection performance indices calculation methods, namely the trip decision method and trip time method respectively. For the trip decision method:

$$PPI_P^E = |D^t - D^r| \quad (5)$$

where:

$$D^t, D^r = \begin{cases} 1 & \text{if relay trips} \\ 0 & \text{otherwise} \end{cases}$$

For the trip time method:

$$PPI_P^E = D^t - D^r$$

where D^t, D^r stand for the trip time of the tested and the referent protection system respectively.

2.4.2 Absolute indices

References [7], [8] and [9] define **security** of protection IED as the ability of the IED to refrain from unnecessary operations. Conversely, **dependability** is the ability of the IED to operate for a fault or abnormal condition within its zone of protection, and they can be defined in mathematical terms as:

$$d = \frac{N_1}{N_{1t}}$$

$$s = \frac{N_0}{N_{0t}}$$

where d is dependability, s is security, N_{1t} is the total number of events for which protection IED should operate, N_1 denotes number of correct trip signals issued, N_{0t} is the total number of events for which IED should restrain from operation and N_0 denotes number of correct trip restraints. These two indices can be combined into the **selectivity** index (see reference [10]) defined as:

$$s = \frac{N_1 + N_0}{N}$$

where N is the total number of exposures.

Other performance indices used in this report are:

- Operating time: average, standard deviation
- Fault location accuracy: defined as the percent difference between the known (simulated) fault location and the value calculated by the relay

2.5 Compatibility Indices

In the context of the all-digital protection system, compatibility means the ability of two or more IEDs to perform their intended functions while sharing the IEC 61850 common communication standard [11]. Interoperability, according to IEC 61850, means the ability of IED from different manufacturers to execute bi-directional data exchange functions in a manner that allows them to operate effectively together [11]. The compatibility evaluation methodology is described in Fig. 2. It will be explained by the following definitions.

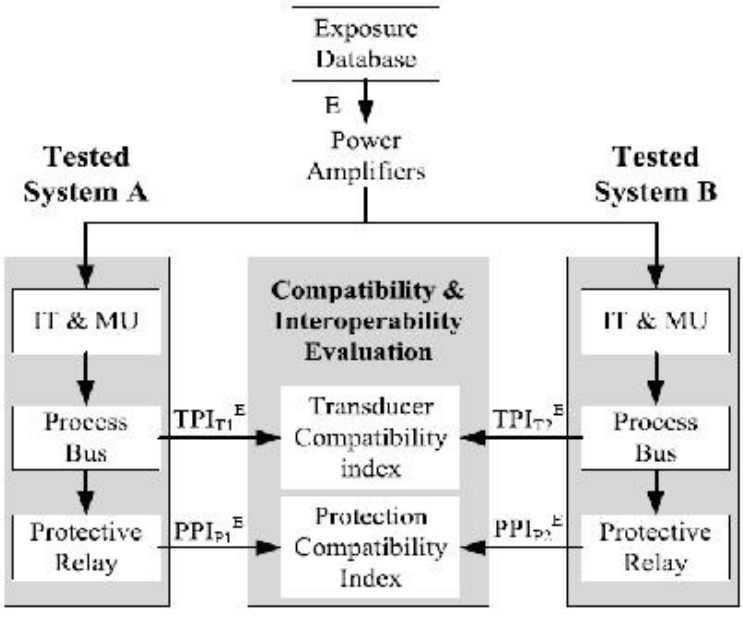

Figure 2. Compatibility indices calculation

Definition 4: *The compatibility index of transducer T1 and T2 when fed by the same test signal E is defined as:*

$$TCI^{E}_{T1,T2}=|TPI^{E}_{T1}-TPI^{E}_{T2}|$$

The average compatibility index of transducer T1 and T2 is defined as:

$$TCI_{T1,T2}=\frac{1}{N}\sum_{E\in EB}|TPI^{E}_{T1}-TPI^{E}_{T2}|$$

The transducer system includes the NCIT and its associated interface electronics (usually referred to as merging unit). By definition, the smaller TCI, the better compatibility and interoperability.

Definition 5: *The compatibility index of protection system P1 and P2 when fed by the same test signal E is defined as:*

$$PCI^{E}_{P1,P2}=|PPI^{E}_{P1}-PPI^{E}_{P2}|$$

The average compatibility index of protection system P1 and P2 is defined as:

$$PCI_{P1,P2}=\frac{1}{N}\sum_{E\in EB}|PPI^{E}_{P1}-PPI^{E}_{P2}|$$

The protection system includes the transducer system, the process bus (the Ethernet LAN) and the protective relay. By definition, the smaller the PCI, the better compatibility and interoperability. Table 1 lists all possible cases for compatibility and interoperability evaluation given that at least two different sets of transducers (T), process bus switches (B) and protective relays (R) are available. To calculate the PCI, we combine the T, B, and R in different protection systems. The possible cases fall into three categories:

1. In the case where compatibility between transducers and relays, and interchangeability between transducers is evaluated, the following compatibility indices can be calculated: $PCI_{P1,P5}$, $PCI_{P2,P6}$, $PCI_{P3,P7}$ and $PCI_{P4,P8}$
2. In the case where interoperability between transducers and IED is evaluated, the following compatibility indices can be calculated: $PCI_{P1,P2}$, $PCI_{P3,P4}$, $PCI_{P5,P6}$ and $PCI_{P7,P8}$
3. In the case where interchangeability between Ethernet switches and/or performance of the protection system with different traffic loads is evaluated, the following compatibility indices can be calculated: $PCI_{P1,P3}$, $PCI_{P2,P4}$, $PCI_{P5,P7}$ and $PCI_{P4,P6}$

It is important to note that all compatibility indices presented in this section can be regarded as relative indices. In other words, values of these indices by themselves serve as an indicator of the difference in compatibility between different systems.

Table 1. Test cases and combinations of protection systems.

Note: T = transducer; B = process bus switch; R = protective relay; P = protection system

T	B	R	P
T1	B1	R1	P1
T1	B1	R2	P2
T1	B2	R1	P3
T1	B2	R2	P4
T2	B1	R1	P5
T2	B1	R2	P6
T2	B2	R1	P7
T2	B2	R2	P8

2.6 Conclusion

This section introduced criteria for evaluation of an all-digital protection system. First, the motivation for defining a methodology that fits the specific needs of an all-digital protection system was discussed. Separate criteria was defined for different evaluation purposes (performance and compatibility indices) as well as for different elements of the protection system (instrument transformers and protective relays). The conclusion of this section is that proposed criteria can be used as a valuable and effective tool to quantitatively determine the performance, compatibility, and interoperability of the novel protection system. The key elements of the methodology are summarized next in the form of questions and answers.

Why the evaluation of an all-digital protection system is necessary and important? The recent development of optical instrument transformers and the advent of microprocessor-based protective relays permit the development of an all-digital protection system based on the IEC 61850 substation communications standard. The performance of the all-digital system has not been investigated in details in the past. Evaluation of the novel digital system should be a significant step towards developing confidence in the application of the new technology in field implementations.

How the difference in performance between an all-digital protection system and a conventional one can be identified? The difference in performance can be measured by defining criteria in the context of transducer and protection system functions. The evaluation can be accomplished by comparing performance of the functions in two cases: 1) A conventional protection system composed of referent instrument transformers and

referent protective relays 2) An all-digital protection system comprised of optical transducers and 61850 compatible protective relays.

What are the means to quantify (measure) the difference? A set of well-defined absolute and relative performance indices has been defined in previous sections. Relative index values are indicators of the mentioned difference, alternatively, absolute index values are NOT indicators of the difference in performance; rather, the DIFFERENCE in values is the indicator.

3.0 Evaluation Methodology

3.1 Introduction

The compatibility indices defined in the previous section, should be calculated by analyzing output signals of transducers and IED from different manufacturers combined into a test system. At least 2 sets of transducers and 2 different protective relays (from one manufacturer) should be available for performing these tests. Availability of one complete test system still allows for calculation of all performance indices defined in previous section. Evaluation system should set as shown on Fig 3.

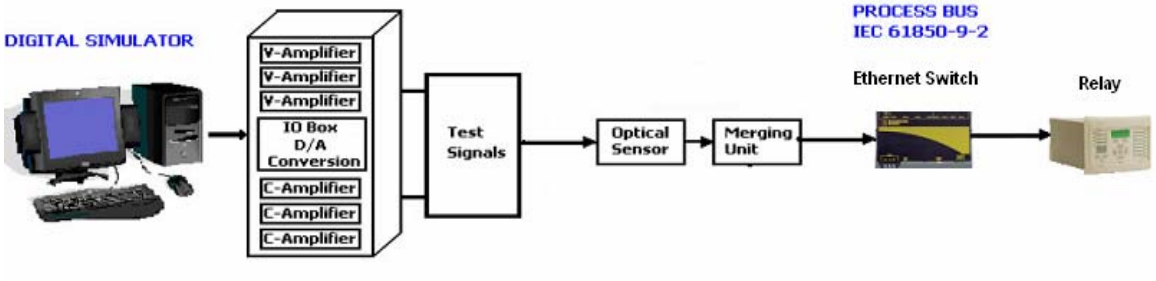

Figure 3. Test setup

Performance indices can be obtained by analyzing the transducer and relay response. Their response is generated by certain input signals. Input signals can be generated from two different sources: 1) Field-recorded data and 2) Simulations

As mentioned in the previous section, exposure signals representing various power system conditions are desirable. Given the typical failure rate of most power system components, it would take many years to collect all the field-data required for this investigation. Hence, simulation is a much more practical approach.

This section describes evaluation through modeling, simulation and lab testing. First, simulation approach will be presented. Second, the power network and protective relay models will be described. Next, simulation scenarios used for generation of all exposure signals will be defined. Finally, details about the hardware architecture as well as the software implementation of the tested systems will be explained.

3.2 Simulation Approach

As mentioned in the introduction, power system responses are triggered by simulated signals corresponding to various power network conditions, such as faults and disturbances. A set of three phase current signals and three phase voltage signals constitutes an exposure. Fig. 4 shows an example of an exposure. The fault type for which this exposure has been recorded is phase-B-to-phase-C-to-ground (BCG) fault, for

a fault located at 20% of the transmission line, without phase-to-phase-to ground resistance. First 8 cycles of the exposure correspond to steady state signals and last 6 cycles are transient post-fault waveforms.

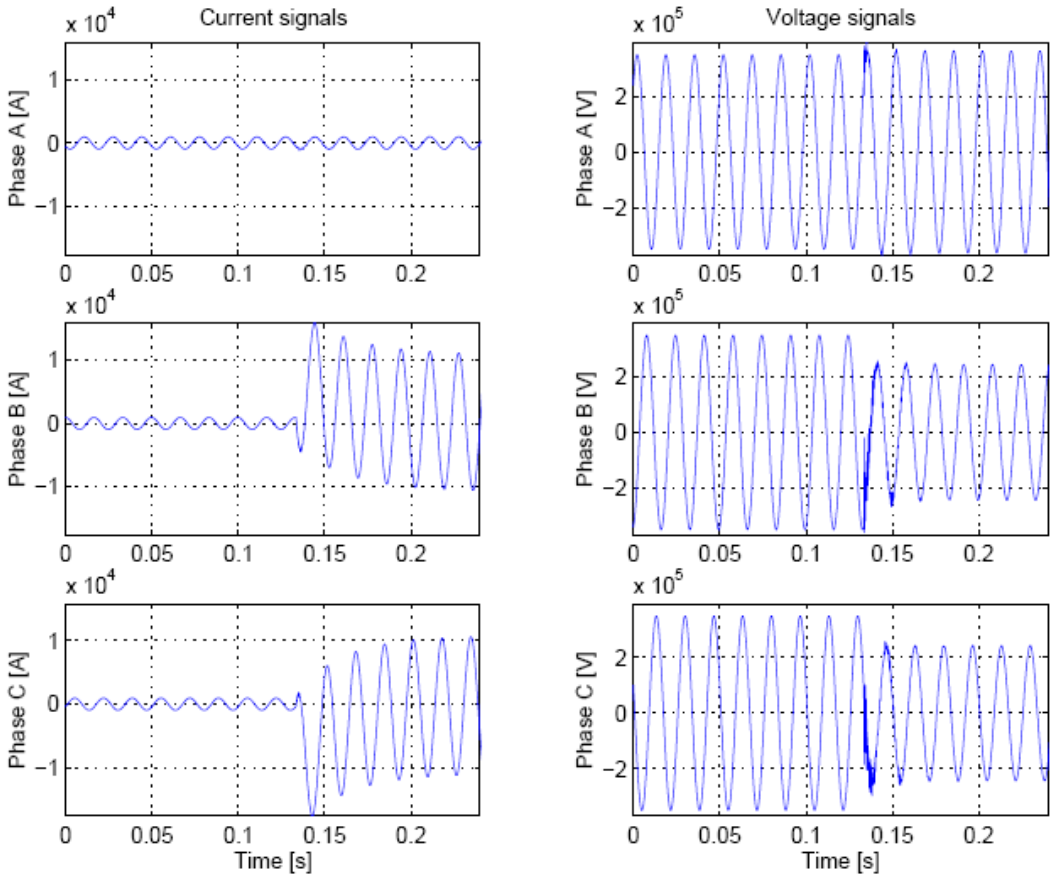

Figure 4. Exposure signals for a BCG fault

The purpose of the simulation and lab testing procedures is to supply the tested protection systems with a large number of exposures and record the transducer and protective relay responses. This process can be summarized as follows:

1. Database of exposures is created by simulating different events using a power network model
2. Exposures are replayed into:
   - All-digital systems assembled in Texas A&M Power Engineering Lab
   - Referent system modeled using ideal instrument transformers and protective relays
3. Output signals from instrument transformers and protective relays are recorded

The steps are illustrated in Fig. 5. Models and scenarios used in simulation are described in the following sections.

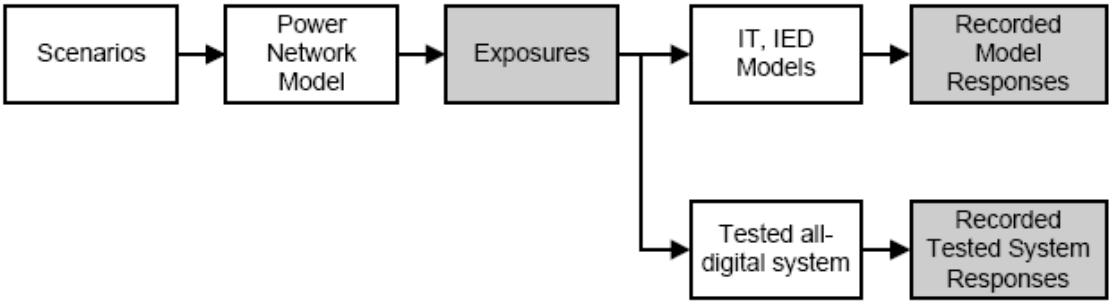

Figure 5. Steps of the simulation process

3.3 Simulation Models

3.3.1 Power network model

The power network model used for simulations is a representation of an actual power system section; the model was developed according to specifications given in [12]. The model offers the flexibility for simulation of various power system conditions and it has been proven to effectively represent dynamic characteristics of disturbances and faults [10], [12]. Remote network sections are modeled using Thevenin equivalents. Fig. 6 shows a one-line diagram of the network.

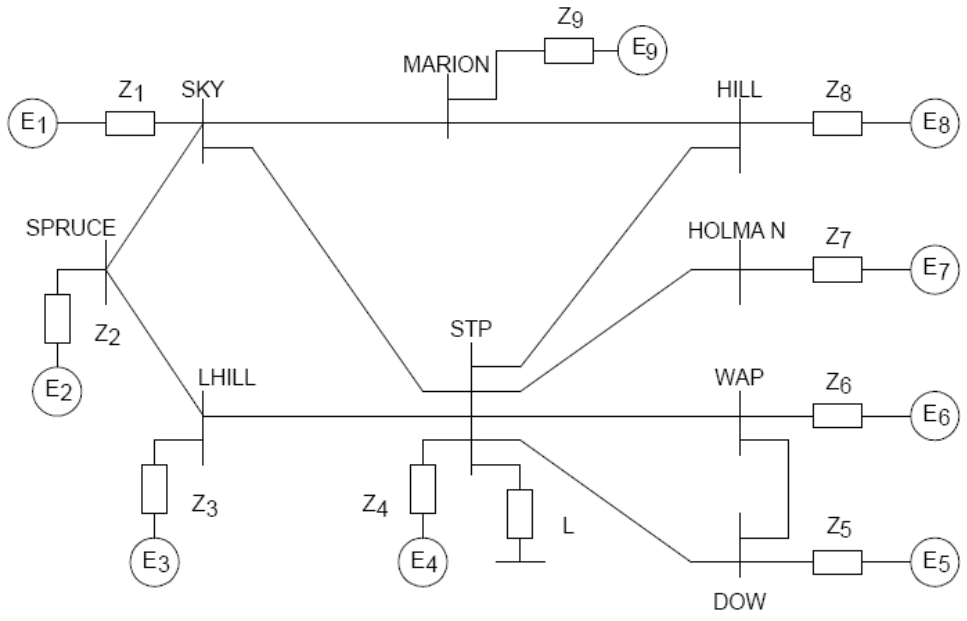

Figure 6. Model of the power network

3.3.2 Relay models

Two relay models were selected for simulation: an overcurrent relay (denoted as model A) and a distance relay (denoted as model B). Both models have been implemented in [5].

Features of the overcurrent relay (model A) are:

- Three-phase directional instantaneous overcurrent protection as primary protection
- Three-phase time overcurrent protection as backup protection
- Residual time overcurrent protection

Functional elements of the model are shown in Figure 7. Elements and their functions are:

- Measuring element extracts current and voltage phasors from the input signals supplied by instrument transformers. Extraction is performed based on Fourier analysis of input signals.
- Overcurrent element consists of 3 sub-elements. Each of the sub-elements implements a certain protection principle. The sub-elements and their functions are:
    1. Time overcurrent protection uses inverse-time characteristic to determine operating time. Time-inverse characteristic allows for fast operation in case of high-level fault currents, and for slow operation in case of low-level fault currents.
    2. Residual time overcurrent protection active only for detection of fault involving ground.
    3. Directional protection determines direction of the flow of the power to determine whether a potential fault is in the direction of protected zone. It restrains assertion of trip command in case of faults in direction opposite to protected zone.
- Logic element performs certain logic functions (AND, OR) to derive trip asserting or trip blocking command at the output of the relay model. The logic is implemented to improve security and dependability of the model.

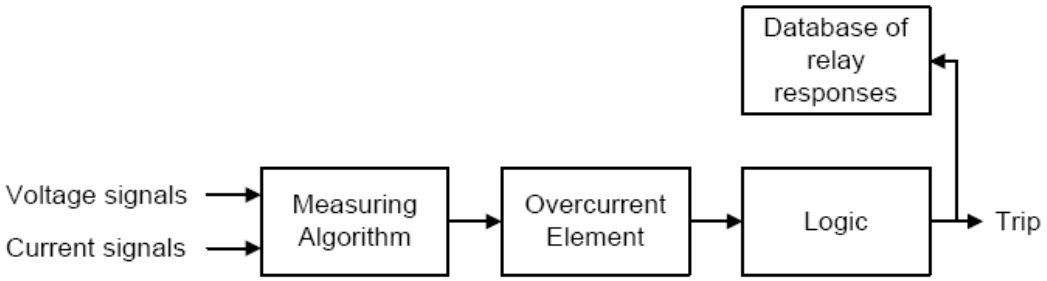

Figure 7. Elements of relay model A

Output signals of the overcurrent relay model (trip decision and tripping time) are recorded and stored in the database of relay responses. Settings of the model are:

- Directional forward protection of the line Sky-STP (see Figure 6.)

- Nominal input current of relay model is I_n=5*A*
- Pickup current is set to 1.5 times the nominal value: I_{pickup}=7.5*A*
- Very inverse time-current characteristic was used. This characteristic is defined as:

$$t_{operate}=\frac{13.5\times k}{I_n\text{-}1}$$

Time-parameter *k* was chosen as: k=0.025. The plot of characteristic is shown in Figure 8.

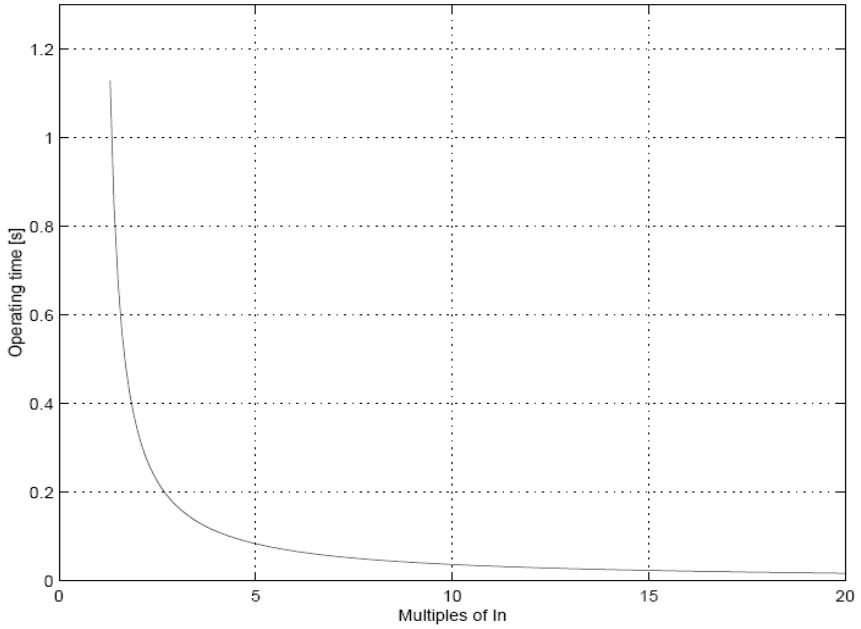

Figure 8. Inverse time-overcurrent characteristic of relay model A

Features of distance relay (model B) are:

- Three separate quadrilateral forward sensing zones for phase to ground faults
- One "quadrilateral" reverse sensing zone for phase to ground faults
- Under voltage element

Functional elements of the model are shown in Figure 9. Elements and their functions are:

- Measuring algorithm extracts impedance from the input current and voltage signals using differential equation algorithm. Impedance from relay location to fault is calculated using expressions for six fault types: AG, BG, CG, ABC, BC, CA.
- Fault identification element determines whether calculated impedance falls into any of the user-defined zones of protection.
- Fault classification element determines fault type, based on impedance calculated for eleven basic fault types.
- Logic element performs certain logic functions to derive trip asserting or trip restraint command at the output of the relay model.

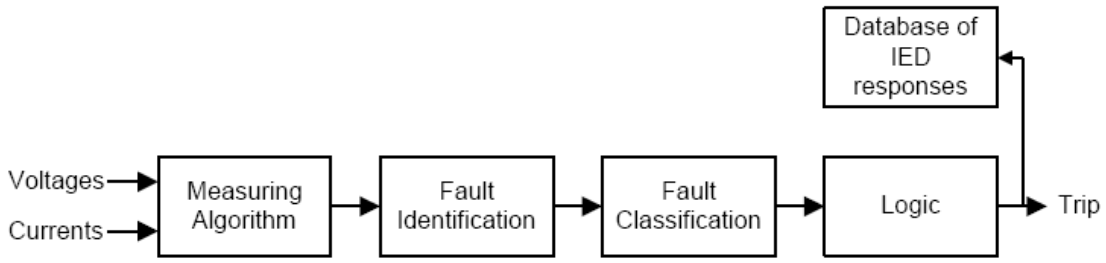

Figure 9. Elements of relay model B

Output signals of distance relay model (trip decision and tripping time) are also recorded and stored in the database of relay responses. Settings of the model are:

- Line under protection is Sky-STP
- Two zones of protection are defined:
    1. First zone covers 80% of the Sky-STP line. This zone is an instantaneous trip zone.
    2. Second zone covers 80% through 120% length of the Sky-STP line. Time delay for this zone is set to 150ms.

- The selected operating characteristic is quadrilateral. Coverage of protection zones and corresponding line impedance are shown in the impedance plane in Figure 10.

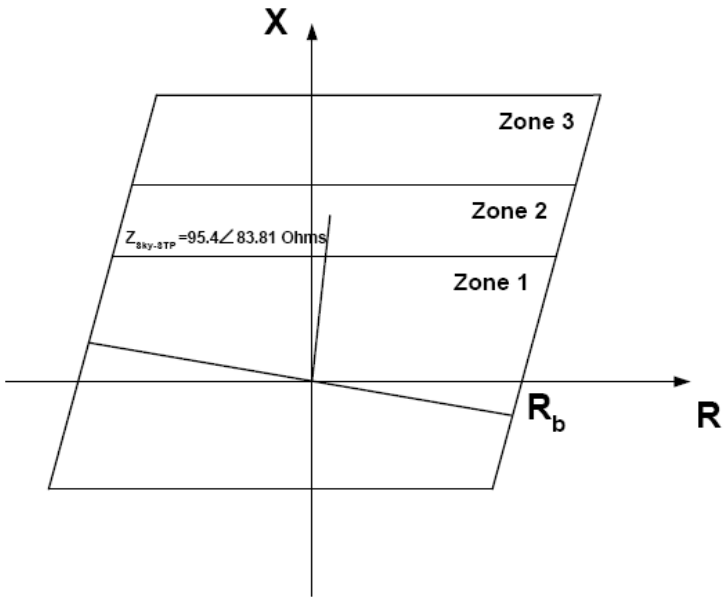

Figure 10. Coverage of quadrilateral zones of the relay model B

3.4 Simulation Scenarios

Simulation scenarios define the power system events to be created and replayed into the modeled referent protection systems and the all-digital protection system assembled in the lab. These events are simulated using a sequence of circuit breaker switching corresponding to various power system conditions. Any particular scenario is defined by two parameters:

- Time at which the event starts and finishes and,

Table 2. Simulation scenario, overcurrent protection

Fault type	Fault Location [%]	Resistance [Ω]	Inception Angle [deg]
AG	-10, 20, 70	0, 5, 10	0, 30, 60, 90
BC	-10, 20, 70	0, 5, 10	0, 30, 60, 90
BCG	-10, 20, 70	0, 5, 10	0, 30, 60, 90
ABC	-10, 20, 70	0	0, 30, 60, 90

- Features of the event, such as: fault location along the transmission line, associated fault resistances (line-to-ground or line-to-line resistance), fault inception angle and fault type.

Table 3. Simulation scenario, distance protection

Fault type	Fault Location [%]	Resistance [Ω]	Inception Angle [deg]
AG	20, 50, 70, 90	0, 5, 10, 20, 30	0, 30, 60, 90
BC	20, 50, 70, 90	0, 5, 10	0, 30, 60, 90
BCG	20, 50, 70, 90	0, 5, 10, 20, 30	0, 30, 60, 90
ABC	20, 50, 70, 90	0	0, 30, 60, 90

Different test scenarios have been defined for the two protection functions to be tested (directional overcurrent and distance protection functions), as shown in Tables 2 and 3. Simulated scenarios are selected to create those power system conditions in which correct operation of the protection system is critical. Overcurrent protection is expected to operate (issuing a trip command) for faults in the forward zone of protection and restraint from operating for faults in the backward zone of operation. Distance protection will be exposed to faults simulated in zones 1 and 2. The relay is expected to operate as a primary protection for faults in zone 1 and backup protection for faults in zone 2.

Four types of fault are simulated: phase-to-ground (AG), phase-to-phase (BC), phase-to-phase-to-ground (BCG) and three phase faults (ABC). In the case of the overcurrent protection testing, three locations along the transmission line are simulated: -10% (backward direction), 20% and 70%. For the distance protection testing, simulated fault locations are: 20%, 50%, 70% and 90%. Number of fault-resistances varies depending on the fault type, for faults involving ground up to 5 different values are used (0Ω, 5Ω, 10Ω, 20Ω, 30Ω) whereas for balanced faults only one is required (0Ω). Finally, every fault is

simulated starting at four different fault inception angles and each fault will be replayed five times into the tested systems.

A total of 120 different exposures (600 tests since each exposure will be replayed 5 times) are generated for the overcurrent protection testing. Also, a total of 224 exposures are created for the distance protection testing (1120 tests).

3.5 Hardware Architecture

The elements and flowchart of the hardware architecture of the test system for all-digital protection system are shown in Fig. 11.

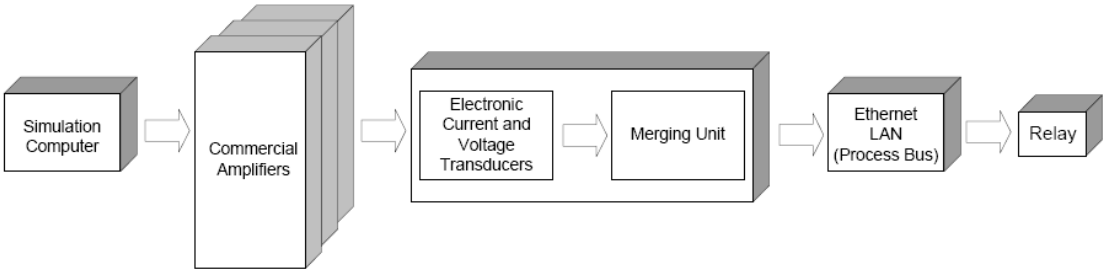

Figure 11. Elements and flowchart of the hardware architecture

Common elements of hardware architecture for all performed tests are:

- Simulation computer: An IBM PC compatible 32-bit personal computer with Windows operating system. Relay Assistant^{TM}, software for open loop transient testing of protective relays, is installed on this computer [13]
- Commercial amplifiers set: consists of three TECHRON TEC3600 single phase voltage amplifiers and three TECHRON TEC7780 single phase current amplifiers interconnected to the simulation computer by a TLI serial communication board (IOBox^{TM}) [14], [15], [16]

Test specific equipment available includes following devices:

- AREVA electronic current transducers set: three phases of magneto optic current sensors [17]
- AREVA electronic voltage transducers set: two kinds of voltage transducers were available. A set of three phases of Pockels cells transducers and a set of three phases of electronic resistive dividers [18]
- AREVA Merging unit: for signal processing, merging and synchronization of signals coming from all electronic current and voltage transducers [17]. It supplies the standardized 61850-9-2 digital interface
- Siemens Hall effect current sensor (one phase)

- Siemens Merging unit: for signal processing, merging and synchronization of signals coming current transducer.
- NxtPhase Optical Current Transducer (one phase)
- NxtPhase Merging unit: for signal processing, merging and synchronization of signals coming current transducer.
- RuggedSwitch^{TM} Ethernet Switch with six 10/100BaseTX ports and two 2-100BaseFX. This is a managed Ethernet switch specifically designed to operate in harsh environments [19].
- GE Multilin Ethernet Switch with 8 10/100BaseTX ports and two 4-100BaseFX. This is a managed Ethernet switch specifically designed to operate in harsh environment
- AREVA Protective relay: MICOM P441 distance relay with two fault detection algorithms, a quadrilateral operating characteristic, backup directional phase overcurrent function and independently settable resistive reach per zone of protection [20].

3.5.1 Test setup description

Based on availability of equipment several different hardware configurations have been tested. Full performance testing, including distance and overcurrent relay functions, was done on one test setup which includes all set of voltage and current sensors, Ethernet switch and Digital Relay. Interoperability of protection system components is first tested by exchanging only Ethernet switches: RUGEDCOM and GE Multilin. Results where almost identical for present level of traffic load and EMI in surrounding area so we decided to test and calculate compatibility indices on three different test setups made by interchanging current sensors only. We were not able to test two or more completely different test setup configurations because of availability of only one digital protective relay AREVA Micom P441.

Interoperability testing is done by testing overcurrent protection function because only one current sensor has been available from all three different vendors. Few non-expected problems happened during lab setup installation process. The first problem related to the availability of sensors. For normal operation relay expects all voltage and current signals from merging unit to be available and valid. In the case when one or more signals from sensors are missing, merging unit will flag those signals as invalid and relay could not operate properly. This problem occurred in TAMU lab because two vendors provided only one current sensor and merging unit to be tested. This problem should be resolved before field deployment because it can lead to misoperation of complete protection system if only one of the sensors fails. For testing purposes, vendors resolved this problem by fixing values of non-existing signals to zero in the merging unit firmware. The second problem was a time-synchronization problem. Merging unit flags all data invalid if good synchronization signal is not available. This could also lead to misoperation of complete protection system if for some reason synchronization fails. It is not uncommon that GPS system fails for short period of time so it is very important that protection system can work without GPS synchronization. Hardware configurations are shown on Figures 12 through 14.

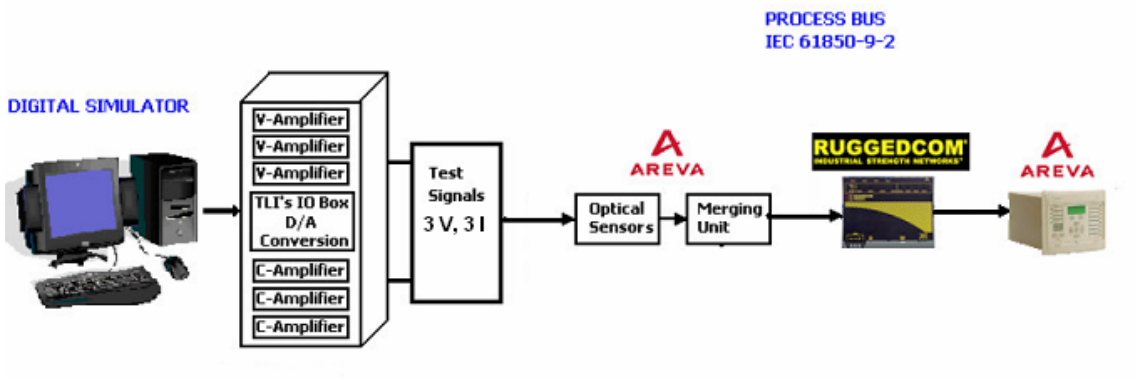

Figure 12. Hardware architecture for Test Setup No. 1

Test setup No. 1: AREVA Optical current sensors and Voltage resistive dividers are connected to Areva Merging Unit providing signal samples in standardized 61850-9-2 digital format. Merging unit is connected to RuggedSwitch Ethernet Switch, which provides data to AREVA MICOM relay that is also connected to Ethernet switch. Communication between sensors and merging unit is implemented using optic fiber cable and vendor's communication protocol. Communication between MU, switch and Relay is IEC 61850-9-2 protocol on cooper Ethernet cable. Test No. 1 setup is shown on Figure 12.

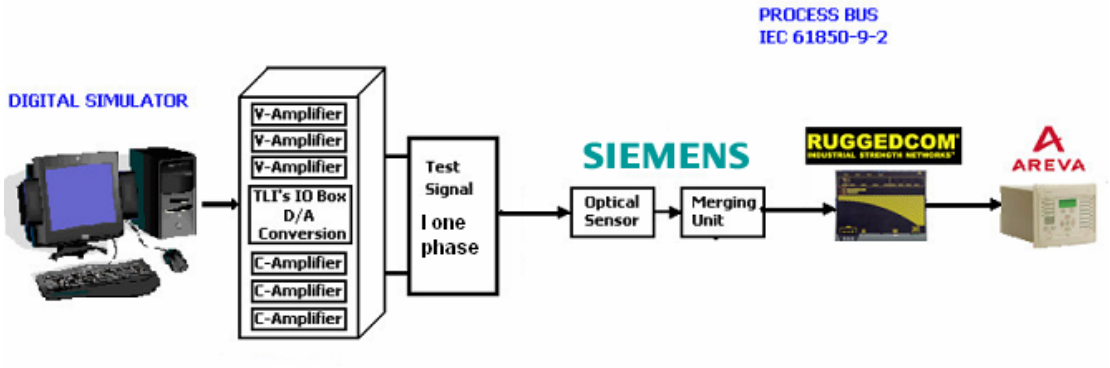

Figure 13. Hardware architecture for Test Setup No. 2.

Test setup No. 2: One NxtPhase current sensor is connected to Merging Unit providing signal samples in standardized 61850-9-2 digital format. Merging unit is connected to RuggedSwitch Ethernet Switch, which provides data to AREVA MICOM relay. Communication between sensor and merging unit is implemented using vendor's optic fiber cable communication. Communication between MU, switch and Relay is IEC 61850-9-2 protocol on cooper Ethernet cable. Test No 2 setup is shown on Figure 13.

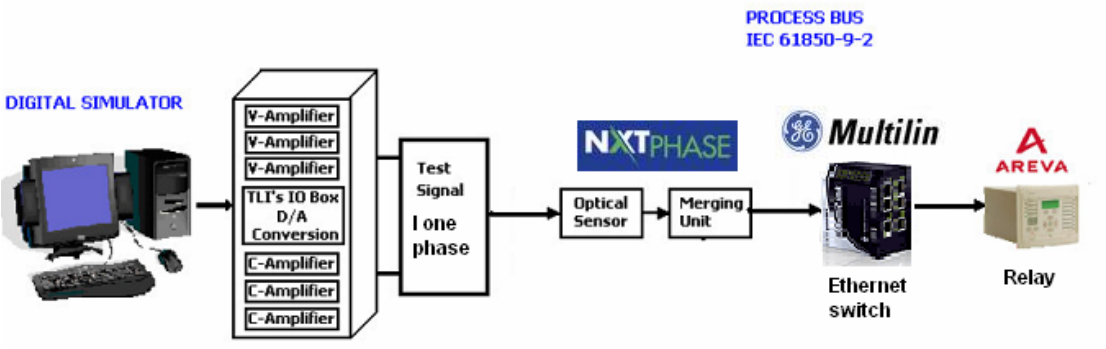

Figure 14. Hardware architecture for Test Setup No. 3.

Test setup No. 3: One Siemens current sensor is connected to Merging Unit providing signal samples in standardized 61850-9-2 digital format. Merging unit is connected to GE Multilin Ethernet Switch, which provides data to AREVA MICOM relay. Communication between sensor and merging unit is implemented using vendor's optic fiber cable communication. Communication between MU and GE switch is realized using IEC 61850-9-2 protocol on optical fiber and communication between switch and relay using IEC 61850-9-2 protocol on cooper Ethernet cable. Test No. 3 setup is shown on Figure 14. The lab setup with all available equipment is shown in Figure 15 as implemented at Texas A&M University Power Engineering Lab.

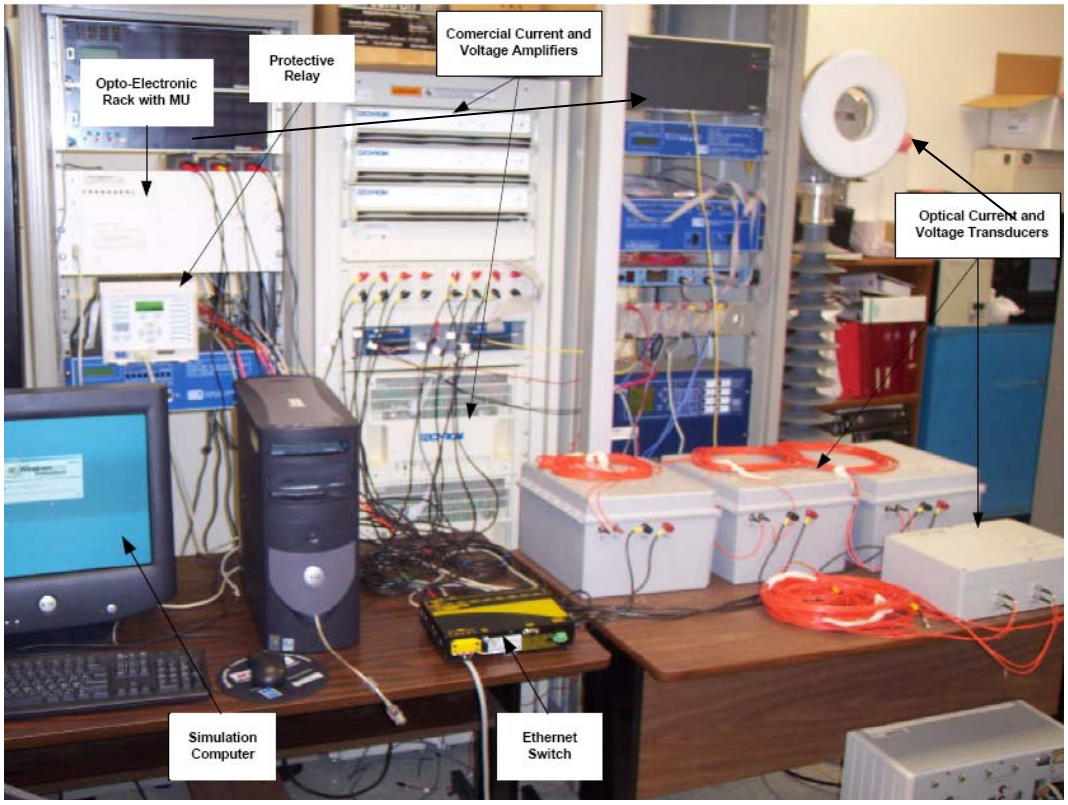

Figure 15. Lab implementation of all-digital protection system

3.6 Software Implementation

The simulation environment consists of several commercial software tools provided for evaluation of the tested all-digital protection system. The simulation environment allows the user to evaluate different power network models, instrument transformers and power system conditions by setting the input_scenario.ini file shown in Figure 16.

```
[System model]
SysModelFile=C:\ProPerformance\models\StpPlain10kHz5sec.atp
SysModelName=Spcspr

[Parameter]
t_prefault=3
t_postfault=15
delta_t=8e-6

[Fault]
FaultType=[AG__]
FaultLoc=[0.20]
FaultRes=[30]
InceptionAngle=[45]
FaultLine=Sky,Stp

[CT model]
CTModelnode1=Sky
CTModelnode2=Stp
CTModelFile=C:\ProPerformance\models\CT02.atp
CTModelName=CT02
CTRatio=900/5
CTBurden=1.3+j*0.175

[VT model]
VTModelnode=Sky
VTRatio=345e3/112
VTBurden=100
VTModelName=VT02
VTModelFile=C:\ProPerformance\models\VT02.atp

[Relay model]
RelayType=D
RelayModelName=R1
RelayModelFile=relay01
RelayPosition=Sky,Stp
```

Figure 16. Example of input data - input scenario file

The input data file specifies six data classes that define all simulation scenarios and models to be evaluated. Elements of the file are:

- System model: location of *.atp version of power network model
- Parameter: timeline of events, represented as the number of cycles of the fundamental frequency for the prefault and postfault portion of the simulated condition

- Fault: fault type, location, resistance and inception angle
- CT model: location of *.atp version of ct model, ct ratio, location on power system model and ct burden
- VT model: location of *.atp version of vt model, vt ratio, location on power system model and vt burden
- Relay model: relay type and location on the power system model

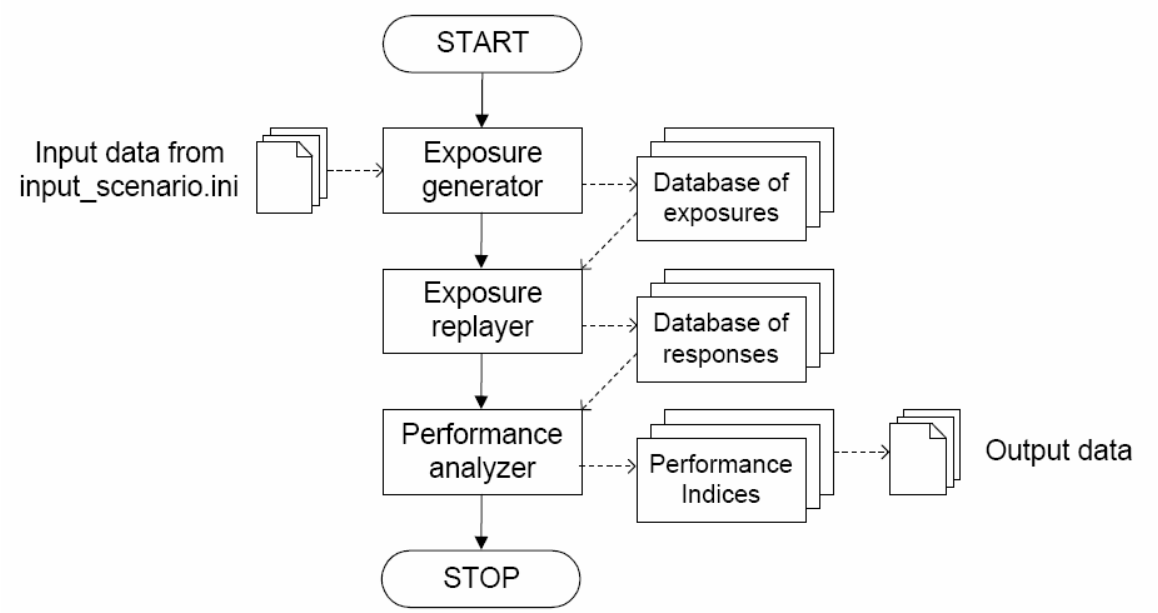

Figure 17. Flowchart of simulation environment

A batch simulation program developed in Matlab [21] has been created based on the *.atp version of power network models (models are implemented in ATP [22] and the choice of the model is made by the user). The program automatically generates a set of exposures for different simulation scenarios with settable parameters as follows: fault type, location, resistance, and inception angle. Output waveforms can be of several formats: PL4, MAT, and COMTRADE [23]. A separate visual C++ software tool has been developed to convert these exposure files from MAT files (Matlab) to RLA (Relay Assistant files).

Simulation environment permits fully automated testing of the referent protection system since software generated models of instrument transformers and protective relays are used. Main functional elements and flowchart of the simulation environment for the evaluation of the referent protection system are shown in Figure 17.

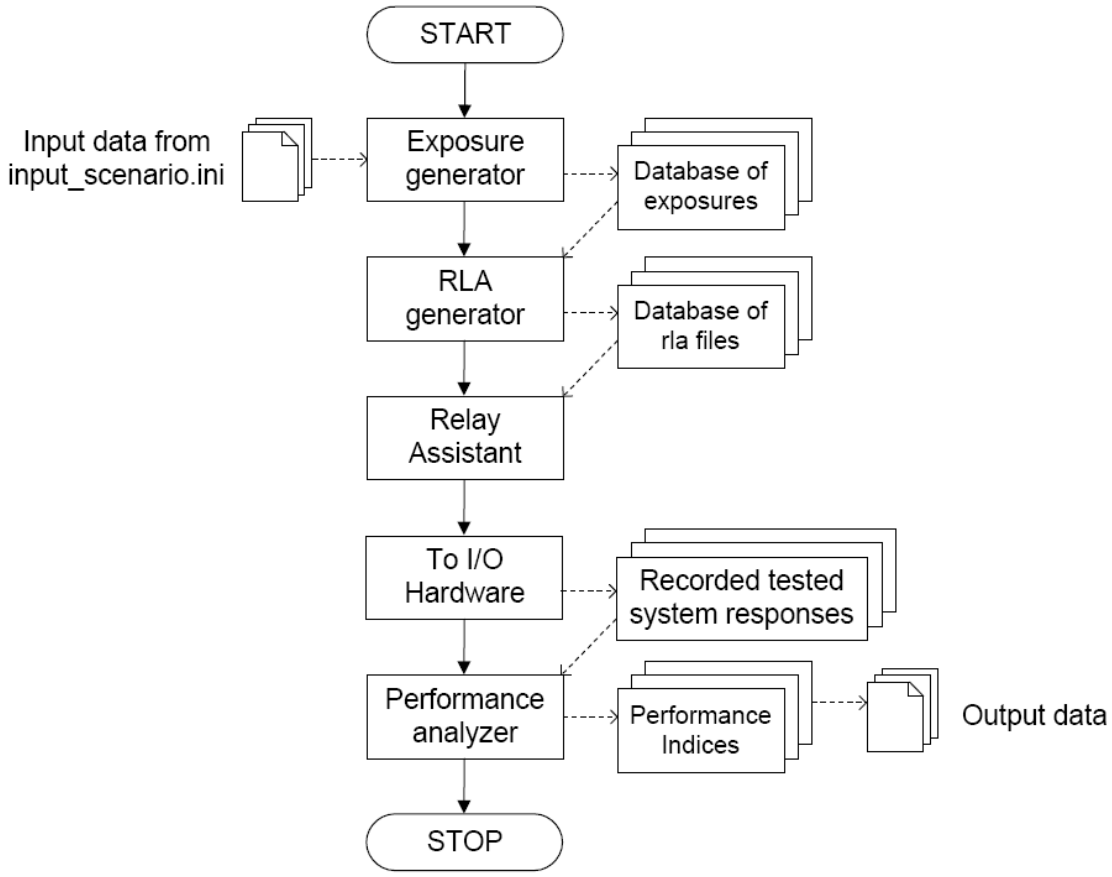

Figure 18. Simulation environment - All-digital system

There are three elements:

- Exposure generator, which uses the input data from input_scenario.ini file to build the database of exposures
- Exposure replayer, in which waveforms from database of exposures are replayed into protective IED models to build database of responses
- Performance analyzer, which uses database of responses to calculate performance indices for the tested protection system

Additional software tools are needed for testing the fully networked all-digital protection system. Simulation environment in this case is partially automated since exposure files are replayed into the tested all-digital system using the Relay Assistant software. The IEC 61850-9-2 digital stream at the process bus level is manually recorded for every test using AREVA's 61850 Digital Analyzer. This software tool allows for visualization of signals from the IEC 61850 protocol. The signals can also be recorded (with settable recording time) and saved to a file. Main elements and flowchart of the simulation environment for the all-digital protection system are shown in Figure 18.

3.7 Conclusion

This section described simulation approach for evaluation of the novel protection system based on an IEC-61850-9-2 digital process bus. First, motivation to combine simulation and lab testing for evaluation purposes was explained. Details of the type of data to be obtained from simulation and procedures to be used are presented. Next, power network and protective relay models are presented. Proper selection of the power system models is required to ensure that both the referent protection system and tested digital protection system are exposed to realistic power system conditions. Also, settings and operating characteristics of relay models used for referent protection system should match those implemented on the 61850 compatible digital relay under evaluation as a part of the tested digital protection system. Selection of features for simulated scenarios was based on the idea that the protection system is best evaluated when exposed to conditions in which correct operation (and interaction) of instrument transformers and protective IED is most critical.

Overall structure of the simulation environment and its software implementation were described. Simulation environment is comprised of several software modules. The four major components of the simulation environment are: 1) exposure generator, 2) exposure replayer, 3) RLA generator and 4) performance analyzer. The main feature of the simulation environment is its adaptability to interface with some other software tools needed for the analysis of the IEC 61850 digital stream. Hardware setups are described and some of the installation problems are mentioned.

Conclusion is that application tests aimed at verifying the behavior of the all-digital protection system can be realized by means of a seamless interaction between the implemented simulation environment and hardware architecture. This section gives the theoretical and practical base for the next section. The next sections present results from simulation and lab testing.

4.0 Methodology Application and Results

4.1 Introduction

This section presents application of the evaluation methodology. Results are obtained by using simulation and test procedure detailed in the previous chapter. Performance indices for the transducer and protective relays of both the referent and tested all digital protection systems are presented in the form of average values. The test system for performance testing was described in previous section. The first section provides values of performance indices for the electronic transducers. Secondly, different types of test performance indices obtained for the different protection system setups are presented. Interoperability of protection system modules is tested and results are presented. Finally, the discussion of test results is given. A summary is given in the last part of this section.

4.2 Electronic Transducer Performance

Output signal from non-conventional instrument transformers can be recorded by means of IEC 61850-9-2 analyzer software as described in the previous chapter. In order to evaluate the values of performance indices for the electronic transducers, it is necessary to define what range of values are indicative of good or "expected" performance and what range of values is indicative of bad or "unexpected" performance. From the definition of the transducer performance indices given in 3, the smaller the value, the better the performance. The following realistic expected values can be used as indication of satisfactory performance:

- TPI_i and TPI_v, which are the time domain transducer performance indices for the current and voltage transducers respectively, should be less than 0.05 (for this value, the accuracy of the transducer system can be regarded to be within 5% when compared to the referent system)
- $TPIF_i$ and $TPIF_v$, which are the frequency domain transducer performance indices for the current and voltage transducers respectively, should also be less than 5%. In both cases the chosen values represent the preferences of the authors based on the knowledge of what each index represents.

4.2.1 Electronic transducers test results

The selection of the values should be done according to the application for which the tested transducer system is being used. The chosen values guarantee accurate performance for protection purposes. Accuracy for metering and energy metering applications should be higher (expected value of both indices could be set to 1% in this case).

Electronic Transducer Performance is performed on Test setup No1, which includes all voltage and current sensors. Values of transducer performance indices are shown in Tables 4 through 7. The following conclusions can be made, based on the performance indices for the electronic transducers:

- Values of time domain and frequency domain performance indices for the tested current transducers indicate a good performance with the exception of values obtained for phase-to-ground faults (AG). The reason for this is the dynamic range of the Faraday sensors used in the evaluation. Faraday sensors are ideally used for sensing high currents (primary rated current ranges from 40 A to 4000 A). The tested Faraday sensors have been modified to measure currents as low as 5 A, which causes the sensor's accuracy to decrease when low currents are simulated (best performance is obtained for ABC faults, which is the fault type that causes higher fault currents, with an average TPI_i of 0.044 and an average $TPIF_i$ of 0.036)
- Values of time domain and frequency domain performance indices for the tested voltage transducers indicate a good performance for all simulated conditions. Values for both performance indices (TPI_v and $TPIF_v$) show very small variations which indicates that they are independent of simulated fault type, location and fault resistance

Table 4. Transducer performance index, ABC fault

Fault Location [%]	**Resistance** [Ω]	TPI_i	$TPIF_i$	TPI_v	$TPIF_v$
20	0	0.039	0.027	0.031	0.006
50		0.046	0.031	0.036	0.007
70		0.046	0.031	0.036	0.009
90		0.045	0.032	0.030	0.008
Average		**0.044**	**0.030**	**0.033**	**0.007**

Table 5. Transducer performance index, AG fault

Fault Location [%]	**Resistance** [Ω]	TPI_i	$TPIF_i$	TPI_v	$TPIF_v$
20	0	0.075	0.065	0.038	0.005
	5	0.079	0.065	0.038	0.005
	10	0.073	0.065	0.028	0.005
	20	0.073	0.065	0.030	0.005
	30	0.073	0.065	0.032	0.004
50	0	0.072	0.064	0.023	0.005
	5	0.073	0.064	0.021	0.005
	10	0.078	0.065	0.043	0.005
	20	0.072	0.065	0.015	0.004
	30	0.073	0.066	0.029	0.004
70	0	0.072	0.065	0.018	0.006
	5	0.074	0.065	0.027	0.006
	10	0.073	0.064	0.016	0.006
	20	0.080	0.064	0.031	0.005
	30	0.079	0.065	0.040	0.006
90	0	0.077	0.064	0.037	0.005
	5	0.076	0.065	0.033	0.005
	10	0.075	0.066	0.026	0.005
	20	0.076	0.067	0.014	0.005
	30	0.084	0.070	0.041	0.004
Average		**0.075**	**0.065**	**0.029**	**0.005**

Table 6. Transducer performance index, BC fault

Fault Location [%]	**Resistance** [Ω]	TPI_i	$TPIF_i$	TPI_v	$TPIF_v$
20	0	0.044	0.035	0.023	0.004
	5	0.048	0.034	0.035	0.004
	10	0.039	0.034	0.014	0.004
50	0	0.049	0.035	0.035	0.005
	5	0.044	0.035	0.021	0.004
	10	0.044	0.035	0.021	0.005
70	0	0.054	0.036	0.039	0.005
	5	0.058	0.036	0.044	0.005
	10	0.050	0.036	0.029	0.005
90	0	0.050	0.038	0.024	0.005
	5	0.053	0.038	0.034	0.005
	10	0.055	0.038	0.034	0.005
Average		**0.049**	**0.036**	**0.029**	**0.005**

Table 7. Transducer performance index, BCG fault

Fault Location [%]	**Resistance [Ω]**	TPI_i	$TPIF_i$	TPI_v	$TPIF_v$
20	0	0.044	0.036	0.020	0.005
	5	0.054	0.032	0.045	0.005
	10	0.045	0.032	0.029	0.005
	20	0.042	0.033	0.023	0.005
	30	0.044	0.033	0.028	0.005
50	0	0.057	0.033	0.040	0.006
	5	0.051	0.034	0.035	0.005
	10	0.043	0.033	0.020	0.005
	20	0.042	0.033	0.021	0.005
	30	0.045	0.033	0.027	0.005
70	0	0.049	0.035	0.026	0.007
	5	0.049	0.035	0.029	0.007
	10	0.045	0.035	0.016	0.006
	20	0.051	0.035	0.030	0.006
	30	0.082	0.068	0.029	0.009
90	0	0.051	0.037	0.024	0.007
	5	0.063	0.037	0.042	0.006
	10	0.077	0.066	0.021	0.005
	20	0.059	0.038	0.039	0.006
	30	0.050	0.037	0.021	0.005
Average		**0.052**	**0.038**	**0.028**	**0.006**

4.3 Protection Performance

Two types of performance indices have been defined to evaluate the performance of the protection system: relative and absolute indices. Results for both kinds of indices have been obtained as methodology was applied to the tested protection functions (overcurrent and distance protection). Full performance testing is done on Test setup No. 1, which includes all voltage and current sensors. The results are presented in the following sections.

4.3.1 Interpretation of relative indices results

The values or relative performance indices, by themselves, are an indication of the DIFFERENCE in performance between the referent protection system and the tested all-digital system. By definition, performance of the referent protection system can be regarded to be ideal, that is, performance has been proven to be accurate and stable in laboratory testing. Since the values of relative indices illustrate a difference in performance, it is necessary to define what range of values are an indication of good or "expected" difference in performance and what range of values is an indication of bad or

"unexpected" difference in performance. The following values can be used for such purpose:

- The average value for PPI_d, which is the trip decision performance index, should be less than 0.02 (a value like this guarantees that trip decision between the two systems is different in less than 2% of the cases)
- The average value for the PPI_t, which is the trip time performance index, should be less than 0.025s or one and a half cycles of the fundamental power system frequency (for a 60 Hz system)

It is important to note that in both cases, the chosen values reflect the preference of the author. Selection of the values was based on typical tripping times for digital relays (see [3] and [24])

4.3.2 Overcurrent protection function test results – Relative indices

This section presents relative indices results obtained by testing protection function of all digital protection system. Two functions are tested: Overcurrent and Distance relay function. Distance function is tested only on Test setup No. 1 because of avilaiability of all set of sensors.

Values of protection performance indices for the overcurrent protection function are shown in Tables 8 through 11.

Table 8. Relative overcurrent protection performance indices, ABC fault

Fault Location [%]	**Resistance [Ω]**	PPI_d	PPI_t
10	0	0	-
20		0	0.019
70		0	0.012
Average		**0**	**0.015**

Table 9. Relative overcurrent protection performance indices, AG fault

Fault Location [%]	**Resistance [Ω]**	PPI_d	PPI_t
10	0	0	-
	5	0	-
	10	0	-
20	0	0	0.021
	5	0	0.020
	10	0	0.019
70	0	0	0.005
	5	0	-0.002
	10	0	-0.011
Average		**0**	**0.009**

Table 10. Relative overcurrent protection performance indices, BC fault

Fault Location [%]	**Resistance [Ω]**	PPI_d	PPI_t
10	0	0	-
	5	0	-
	10	0	-
20	0	0	0.021
	5	0	0.021
	10	0	0.021
70	0	0	0.019
	5	0	0.019
	10	0	0.019
Average		**0**	**0.020**

Table 11. Relative overcurrent protection performance indices, BCG fault

Fault Location [%]	**Resistance [Ω]**	PPI_d	PPI_t
10	0	0	-
	5	0	-
	10	0	-
20	0	0	0.021
	5	0	0.021
	10	0	0.021
70	0	0	0.016
	5	0	0.014
	10	0	0.014
Average		**0**	**0.018**

The following conclusions can be made, based on the performance indices for the overcurrent protection function:

- A PPI_d of zero for all fault types shows there is no difference in the ability of the overcurrent protection function from the tested relay to properly detect the simulated faults when compared to the overcurrent relay model in the referent protection system
- Average values for the PPI_t range between 9 ms for phase-to-ground faults (AG) to 20 ms for phase-to-phase faults (BC). Difference in performance between the tested and referent protection systems is relatively small

4.3.3 Results - Relative indices for distance protection

Values of protection performance indices for the distance protection function are shown in Tables 12 through 15. The following conclusions can be made based on the performance indices for the distance protection function:

- As in the case of the overcurrent protection, an average value for the PPI_d of 0.009 shows that performance of the fault detection algorithm for the IEC 61850 compatible distance protective relay is very similar to performance obtained from the distance relay model. Only in two cases the tested distance relay failed to issue a trip command (fault location at 50% of the line and fault resistance of 30 Ω)
- By looking at the average values for the PPI_t (it ranges from 27 to 38 ms), it is obvious that tripping times for the tested digital distance relay differ significantly from those obtained from the distance relay model in the referent protection system. This is due in most part by longer processing times of the decision making algorithm inside the tested relay. For some simulated AG faults (with fault resistance of 20 and 30 Ω) the tested distance protection issued trip commands with incorrect time delay (faults in primary zone detected as belonging to backup zone). This last factor influencing the operating time of the tested distance relay will be discussed in the next sections

Table 12. Relative distance protection performance indices, ABC fault

Fault Location [%]	**Resistance [Ω]**	PPI_d	PPI_t
20	0	0	0.031
50		0	0.050
70		0	0.046
90		0	0.023
Average		**0**	**0.038**

Table 13. Relative distance protection performance indices, AG fault

Fault Location [%]	**Resistance [Ω]**	PPI_d	PPI_t
20	0	0	0.017
	5	0	0.015
	10	0	0.020
	20	0	0.027
	30	0	0.104
50	0	0	0.018
	5	0	0.025
	10	0	0.023
	20	0	0.116
	30	0.5	-
70	0	0	0.011
	5	0	0.011
	10	0	-0.060
	20	0	-
	30	0	-
90	0	0	0.019
	5	0	0.030
	10	0	-
	20	0	-
	30	0	-
Average		**0.025**	**0.027**

Table 14. Relative distance protection performance indices, BC fault

Fault Location [%]	**Resistance [Ω]**	PPI_d	PPI_t
20	0	0	0.030
	5	0	0.032
	10	0	0.031
50	0	0	0.040
	5	0	0.038
	10	0	0.039
70	0	0	0.053
	5	0	0.037
	10	0	0.047
90	0	0	0.030
	5	0	0.030
	10	0	0.027
Average		**0**	**0.036**

Table 15. Relative distance protection performance indices, BCG fault

Fault Location [%]	**Resistance [Ω]**	PPI_d	PPI_t
20	0	0	0.032
	5	0	0.029
	10	0	0.026
	20	0	0.026
	30	0	0.027
50	0	0	0.029
	5	0	0.025
	10	0	0.029
	20	0	0.027
	30	0	0.027
70	0	0	0.027
	5	0	0.025
	10	0	0.029
	20	0	0.026
	30	0	0.027
90	0	0	0.016
	5	0	0.026
	10	0	0.030
	20	0	0.035
	30	0	0.030
Average		**0**	**0.027**

4.3.4 Absolute indices for overcurrent protection function

Even though general criteria and definition of absolute performance indices has been detailed in section 3, further clarification of the indices from the overcurrent protection perspective is needed.

- s_1 is defined as:

$$s_1 = \frac{N_1}{N_{forward}}$$

- s_2 is defined as:

$$s_2 = \frac{N_2}{N_{backward}}$$

where: N_1 is the number of correct trip assertions for faults in forward direction and N_2 is the number of correct trip restrains for faults in backward direction.

$N_{forward}$ and $N_{backward}$ are the number of faults simulated in the forward and backward zones of protection respectively

- t is the average tripping (operating) time
- σ is the standard deviation for the recorded tripping times, which is a common measure of statistical dispersion

4.3.5 Overcurrent protection function test results - Absolute indices

This section presents absolute indices results obtained by testing protection function of all digital protection system. Two functions are tested: Overcurrent and Distance relay function. Distance function is tested only on one setup of equipment for the same reason.

Values of protection performance indices for the overcurrent protection function are shown in Tables 16 through 19.

The following conclusions can be made, based on the results:

- Selectivity of overcurrent protection function for the tested all-digital protection system is perfect. In all of the simulated faults the relay correctly issued trip commands for faults in forward zone and restrained from operation for faults in backward zone
- A comparison of the average tripping times shown in Tables 16 through 19 demonstrates that for all simulated fault types the reaction time of the tested relay is very close to the expected operating time given by the very inverse time-current characteristic presented in section 3
- Average values for the standard deviation (it ranges from 0.002 to 0.003) show that there is a high degree of certainty that the tested digital relay's operating time for any given fault will consistently follow the operating time-current characteristic with almost a negligible level of dispersion from the mean trip time (around 2 ms)

Table 16. Absolute overcurrent protection performance indices, ABC fault

Fault Location [%]	**Resistance [Ω]**	s_1	s_2	$t[s]$	$\sigma[s]$
10	0	-	1	-	-
20		1	-	0.052	0.003
70		1	-	0.098	0.002
Average		**1**	**1**	**0.075**	**0.002**

Table 17. Absolute overcurrent protection performance indices, AG fault

Fault Location [%]	**Resistance [Ω]**	s_1	s_2	$t[s]$	$\sigma[s]$
10	0	-	1	-	-
	5	-	1	-	-
	10	-	1	-	-
20	0	1	-	0.076	0.002
	5	1	-	0.079	0.002
	10	1	-	0.081	0.002
70	0	1	-	0.194	0.003
	5	1	-	0.208	0.003
	10	1	-	0.230	0.003
Average		**1**	**1**	**0.0145**	**0.003**

Table 18. Absolute overcurrent protection performance indices, BC fault

Fault Location [%]	**Resistance [Ω]**	s_1	s_2	$t[s]$	$\sigma[s]$
10	0	-	1	-	-
	5	-	1	-	-
	10	-	1	-	-
20	0	1	-	0.058	0.002
	5	1	-	0.058	0.002
	10	1	-	0.057	0.002
70	0	1	-	0.109	0.003
	5	1	-	0.109	0.003
	10	1	-	0.109	0.004
Average		**1**	**1**	**0.083**	**0.003**

Table 19. Absolute overcurrent protection performance indices, BCG fault

Fault Location [%]	Resistance [Ω]	s_1	s_2	$t[s]$	$\sigma[s]$
10	0	-	1	-	-
	5	-	1	-	-
	10	-	1	-	-
20	0	1	-	0.057	0.002
	5	1	-	0.057	0.001
	10	1	-	0.056	0.002
70	0	1	-	0.110	0.001
	5	1	-	0.112	0.002
	10	1	-	0.114	0.003
Average		**1**	**1**	**0.084**	**0.002**

4.3.6 Distance protection function test results - Absolute indices

Values of protection performance indices for the distance protection function are shown in Tables 20 through 23. Meaning of indices is explained next:

- s_1 is defined as: $s_1 = \frac{N_1}{N_{primary}}$
- s_2 is defined as: $s_2 = \frac{N_2}{N_{backup}}$

  where: N_1 is the number of correct trip assertions for faults in the primary zone of protection and N_2 is the number of correct trip assertions for faults in the backup zone of protection. $N_{primary}$ and N_{backup} are the faults simulated in the primary and backup zones of protection respectively
- Fault location error, FL_{err}, defined as:

  $$FL_{err} = \frac{|measured\text{-}actual|}{actual} \times 100\%$$

  where: *measured* refers to the fault location calculated by the relay and *actual* refers to the known (simulated) fault location
- t_1 and t_2 is the average tripping (operating) time for the primary and backup zones of protection respectively

The following conclusions can be made, based on the results:

- Selectivity was very good for all fault types with the exception of phase-to-ground faults (AG). Selectivity for AG faults was low (0.71 for primary zone and 0.4 for backup zone) due to the relay's inability to detect high-resistance faults (relay did not trip for faults at 50% with a fault resistance of 30 Ω, faults at 70% with 20 or

30 Ω and faults at 90% with 10 - 30 Ω), or in some cases, due to trip assertions with incorrect time delay for faults in the primary zone of protection. Usually, distance relays are not sensitive enough to detect these high resistance faults, specially for phase-to-ground faults, that is why sensitive ground overcurrent protection is used in addition to the distance protection (typically, both functions are available in the same protective IED)

- Average tripping time for the primary zone of protection is within the expected values (it varies from about 2 cycles for BCG faults to 3 cycles for an AG fault). Also, considering a set time delay of 150 ms for backup zone of protection, average tripping times for the backup zone are also within the expected range (it ranges from 171 to 178 ms)
- Values for the standard deviation show that for almost all fault types (excluding BCG faults) the tripping times are usually far from the average tripping time. This means that for any given event, there will be little certainty to whether the relay's operating time will be close to the expected (mean) value. Since the collected data approximates to a normally distributed population (verified through a normal probability plot), it can be assumed that about 68% of the value are within 1 standard deviation of the mean. Applying this to the BC fault type, 68% of the recorded tripping time for the primary zone should be between 29 and 71 ms. This also means that approximately 16% of the tripping times will be higher than 71ms (the actual value was 15% for BCG faults), which is an unacceptably high operating time for a trip in zone I.
- The average fault location error is tolerable (around 5%) for all simulated conditions with the exception of those obtained for BC and BCG faults located at 20% of the transmission line. In these cases, average fault location error ranges from 13 to 23%. As it was previously explained, for most single phase-ground faults simulated at 20 and 50% of the line, the high fault resistance caused the distance protection to incorrectly sense faults within its primary zone of protection, as being outside of the reach. This had an effect on the fault locator's estimation and explains unexpected values for the FL_{err} in this cases

Table 20. Absolute distance protection performance indices, ABC fault

Fault Location [%]	**Resistance** [Ω]	s_1	s_2	$t_1[s]$	$t_2[s]$	$\sigma[s]$	$FL_{err}[\%]$
20	0	1	-	0.039	-	0.019	3.07
50		1	-	0.061	-	0.031	6.83
70		1	-	0.061	-	0.031	4.65
90		-	1	-	0.171	0.028	6.58
Average		**1**	**1**	**0.054**	**0.171**	**0.027**	**5.28**

Table 21. Absolute distance protection performance indices, AG fault

Fault Location [%]	**Resistance [Ω]**	s_1	s_2	$t_1[s]$	$t_2[s]$	$\sigma[s]$	$FL_{err}[\%]$
20	0	1	-	0.035	-	0.012	3.99
	5	1	-	0.033	-	0.016	4.80
	10	1	-	0.039	-	0.011	7.91
	20	1	-	0.048	-	0.015	12.65
	30	0.35	-	0.123	-	0.072	18.46
50	0	1	-	0.043	-	0.010	2.78
	5	1	-	0.050	-	0.018	6.16
	10	1	-	0.049	-	0.021	9.17
	20	0.3	-	0.142	-	0.079	16.04
	30	0	-	-	-	-	-
70	0	1	-	0.045	-	0.012	4.28
	5	1	-	0.048	-	0.016	7.68
	10	1	-	0.061	-	0.028	10.98
	20	0	-	-	-	-	-
	30	0	-	-	-	-	-
90	0	-	1	-	0.168	0.026	3.83
	5	-	1	-	0.179	0.020	14.85
	10	-	0	-	-	-	-
	20	-	0	-	-	-	-
	30	-	0	-	-	-	-
Average		**0.71**	**0.4**	**0.057**	**0.173**	**0.020**	**8.69**

Table 22. Absolute distance protection performance indices, BC fault

Fault Location [%]	**Resistance [Ω]**	s_1	s_2	$t_1[s]$	$t_2[s]$	$\sigma[s]$	$FL_{err}[\%]$
20	0	1	-	0.038	-	0.011	13.67
	5	1	-	0.041	-	0.013	15.11
	10	1	-	0.040	-	0.014	16.89
50	0	1	-	0.051	-	0.020	3.24
	5	1	-	0.050	-	0.021	3.80
	10	1	-	0.051	-	0.014	2.39
70	0	1	-	0.067	-	0.024	4.18
	5	1	-	0.051	-	0.020	3.67
	10	1	-	0.061	-	0.029	3.89
90	0	-	1	-	0.179	0.038	4.92
	5	-	1	-	0.179	0.029	5.69
	10	-	1	-	0.176	0.021	5.91
Average		**1**	**1**	**0.050**	**0.178**	**0.021**	**6.95**

Table 23. Absolute distance protection performance indices, BCG fault

Fault Location [%]	**Resistance [Ω]**	s_1	s_2	$t_1[s]$	$t_2[s]$	$\sigma[s]$	$FL_{err}[\%]$
20	0	1	-	0.041	-	0.010	17.08
	5	1	-	0.037	-	0.010	20.26
	10	1	-	0.034	-	0.013	22.90
	20	1	-	0.035	-	0.012	13.14
	30	1	-	0.036	-	0.012	21.39
50	0	1	-	0.040	-	0.008	3.26
	5	1	-	0.036	-	0.009	2.87
	10	1	-	0.040	-	0.008	3.08
	20	1	-	0.038	-	0.008	3.34
	30	1	-	0.038	-	0.009	4.64
70	0	1	-	0.042	-	0.008	4.19
	5	1	-	0.040	-	0.009	8.90
	10	1	-	0.043	-	0.014	4.06
	20	1	-	0.040	-	0.008	6.46
	30	1	-	0.041	-	0.013	4.32
90	0	-	1	-	0.166	0.017	5.47
	5	-	1	-	0.174	0.016	9.24
	10	-	1	-	0.177	0.016	4.79
	20	-	1	-	0.181	0.022	4.39
	30	-	1	-	0.176	0.018	4.62
Average		**1**	**1**	**0.039**	**0.175**	**0.012**	**8.42**

4.4 Compatibility and Interoperability

Compatibility indices have been defined to evaluate the ability to interchange parts of the protection system. Results for compatibility indices have been obtained as methodology was applied to the tested protection systems. Interoperability testing is done comparing performances of three test setups. The results are presented in the following sections.

4.4.1 Interpretation of compatibility indices results

The values of compatibility indices show the DIFFERENCE in performance between the two all-digital protection systems. By definition, the smaller compatibility indices, the better compatibility and interoperability of two systems. Ideally, compatibility should be equal to zero. This means that two systems have the same performance if compatibility indices are close to zero.

These indices as they are defined in previous section describe average difference in all-digital protection systems performance. First, in the next section we will present performance indices of overcurrent protection function tested on all three test setups in the same conditions.

4.4.2 Performance results of overcurrent protection function

Absolute performance indices for all three test setups are presented. All performance indices results shown in this section are calculated as it is described in previous sections. Values of protection performance indices for all three test setups are shown in Tables 24 through 26 respectively.

Table 24. Absolute overcurrent performance indices, Test setup No. 1

Fault Type	Fault Location	S	Average t[s]	Average σ[s]
AG	20	1	0.0793	0.002
	70	1	0.3253	0.002
BC	20	1	0.0573	0.002
	70	1	0.1766	0.003
BCG	20	1	0.0503	0.003
	70	1	0.145	0.002
ABC	20	1	0.049	0.002
	70	1	0.121	0.002

Table 25. Absolute overcurrent performance indices, Test setup No. 2

Fault Type	Fault Location	S	Average t[s]	Average σ[s]
AG	20	1	0.0787	0.002
	70	1	0.3210	0.002
BC	20	1	0.0543	0.001
	70	1	0.1673	0.002
BCG	20	1	0.0480	0.002
	70	1	0.1427	0.003
ABC	20	1	0.0490	0.001
	70	1	0.1200	0.002

Table 26. Absolute overcurrent performance indices, Test setup No. 3

Fault Type	Fault Location	S	Average t[s]	Average σ[s]
AG	**20**	**1**	**0.0750**	**0.002**
	70	**1**	**0.3110**	**0.003**
BC	**20**	**1**	**0.0580**	**0.002**
	70	**1**	**0.1587**	**0.002**
BCG	**20**	**1**	**0.0517**	**0.002**
	70	**1**	**0.1377**	**0.003**
ABC	**20**	**1**	**0.0520**	**0.001**
	70	**1**	**0.1140**	**0.002**

The following conclusions can be made, based on the results:

- Selectivity of overcurrent protection function for the tested all-digital protection systems is perfect.
- A comparison of the average tripping times shown in Tables 24 through 26 demonstrates that for all simulated fault types the reaction times of the tested systems are very close to each other.
- Average values for the standard deviation show that there is a high degree of certainty that the tested digital protection system's operating time for any given fault will be consistent.

4.4.3 Interoperability results

Compatibility indices which describe interoperability between all three tested protection systems are presented. Indices are calculated as it is described in previous sections. Results for all possible combinations of the tested setups are given in Table 27.

Table 27. Interoperability test results

Tests	1st Test Setup (CT+MU - Eth. Switch - Relay)	2nd Test Setup (CT+MU - Eth. Switch - Relay)	Average trip time	PCI
I - II	AREVA – RUGGEDCOM – AREVA	NxtPhase – RUGGEDCOM – AREVA	0.12405	0.0024
II - III	NxtPhase – RUGGEDCOM – AREVA	Siemens – GE Multilin – AREVA	0.12119	0.00758
I - III	AREVA – RUGGEDCOM – AREVA	Siemens – GE Multilin – AREVA	0.12262	0.00645

The following conclusions can be made, based on the results:

- Comparison between average tripping times for all systems are very close to each other.
- Compatibility indices which describes performance difference between given systems are relatively small
- Parts of the tested systems can be interchanged without significant effect to system performance.

4.5 Conclusion

Results from the performance evaluation of an all-digital protection system based on an IEC-61850-9-2 process bus are presented in this chapter. Results were obtained by application of the evaluation criteria described in section 3. Application tests were performed using the hardware architecture (lab setup) presented in 4 and the software implementation detailed in the same section. The following comments can be made, based on the results from application testing:

- Non-conventional instrument transducers, based on new sensing technologies, showed excellent performance for all simulated power system conditions. Values of transducer performance indices (for both, time and frequency domain) indicate that current and voltage transducers based on new sensing technologies deliver nearly distortion-free replicas of signals from their primary side. By keeping the distortion to acceptable levels, it is possible to guarantee that performance of protection system IED will not be affected or influenced by unacceptable transducer performance
- Difference in performance between the novel (all-digital) and referent protection systems varies considerably from one protection function (operating principle) to another. For the overcurrent protection function there is no significant difference in performance with respect to trip decision and average tripping time. Average operating times for the all-digital distance protection are considerably higher than those of the distance relay model.
- Relative indices provide a simple and effective way to measure the overall performance of the tested system against a selected referent system. Many protective relays compatible with IEC 61850-9-2 are expected to become commercially available in the near future and comparison of different systems will be highly desirable
- Performance of the novel system can be regarded as excellent when considering test results for the directional overcurrent protection function. Relevance of this result lies in the fact that these two principles (comparison of the measured quantity versus a threshold and distinction of current flow) are the basis for many other protection functions
- Problematic performance of the distance protection function, with respect to the operating time, was confirmed by means of absolute performance indices. Although average operating times are within the expected values, results show

there is great uncertainty with respect to what tripping time can be expected for any given event, which means calculated average tripping times are not necessarily a good prediction of the relay's reaction time

- High fault location estimation errors only for faults of a certain type and at a certain location (phase-to-phase faults that are close to the relay's location, in this case, 20% of the line) show how these behaviors can be hard to detect using traditional test procedures or field-data. A flexible and automated simulation environment combined with the available lab setup is a powerful tool to identify and correct problems during the design stage of the device
- Overall protection system performance in not affected by interchange of Ethernet switches. For the present level of traffic load on the process bus and low level of EMI in the lab difference in performance indices were negligible. Ethernet switch interoperability should be tested in harsh environment with the high level of traffic load.
- Overcurrent performance indices for systems composed by interchanging sensors and merging units are very similar. Testing based on the same input signals and relay setting data shows that there is no significant difference in protection system performance.
- Low interoperability indices shows that tested protection systems are compatible and can be interchanged without significant effect on protection system performance. Sensors and merging units interchanged during these tests have almost the same performance characteristics.

5.0 Conclusion

5.1 Summary

This report presents evaluation criteria and methodology for performance evaluation of all-digital systems. Criteria and methodology for numerical evaluation of the all-digital protection system is defined in section 3. Separate criteria were defined for different evaluation purposes (performance and compatibility) and for performance evaluation of different system components. Proposed criteria pursue to answer three important questions pertinent to the evaluation of the novel system: 1) Why the evaluation is necessary? 2) How the difference in performance between the novel and conventional protection systems can be identified and quantified? And 3) How the compatibility and interoperability between the all-digital protection systems can be identified and quantified?

Evaluation approach through modeling, simulation and lab testing was described in section 4. Simulation approach was presented, along with simulation models (power network and relay models) and different simulation scenarios. Next, details of hardware architecture used for the process bus implementation were given. Finally, the software implementation, consisting of the developed simulation environment and several third party software tools, was discussed. It was concluded that application tests required to test the behavior of the novel digital system can be realized by means of a seamless interaction between the implemented simulation environment and hardware architecture.

Application of the evaluation methodology was presented in Chapter 5. Results are definitely helpful in gaining understanding on what level of performance can be expected from the novel system, how does the measured performance compares to that of conventional systems and to each other, what elements of the novel system contribute to problematic performance and under what conditions. It was concluded that:

- Non-conventional instrument transformers are not expected to influence the performance of protection IED since they deliver replicas of signals from their primary side with a relatively small distortion level.
- Problematic behavior of certain protection functions in the all-digital system can be easily identified by analyzing numerical values of performance indices.
- Compatibility and interoperability of all-digital protection systems are demonstrated and results show that systems can perform similarly regardless of equipment vendor selection.

5.2 Research Contribution

Performance and compatibility of an all-digital protection system was not investigated in details in the past. Two main reasons for this are: 1) IEC 61850-9-2 compatible devices have just recently been made available for lab test purposes and 2) there was no systematic methodology to assess the feasibility and evaluate the overall performance of the novel system. Both issues have been addressed in this investigation. Major contributions of this report are:

- Criteria and methodology for performance and compatibility evaluation of an all-digital protection system, consisting of non-conventional instrument transformers interfaced to digital relays via an IEC 61850-9-2 digital process bus. In the case of performance evaluation, criteria have been defined in the form of two types of numerical indices, namely relative and absolute performance indices. The first type provides an indication of the DIFFERENCE in performance between the tested all-digital system and a referent protection system. The second type offers a quantitative indication of the performance of the tested system only.
- Feasibility of the all-digital system has been demonstrated by the successful application of the mentioned methodology to the lab setup assembled in Texas A&M University's Power Engineering Lab Hardware architecture can be easily expanded to investigate some other technical aspects of interest within the novel system, such as absolute synchronization of sampled values.
- Criteria and methodology have been applied through the software implementation. It was shown that the proposed approach is a valuable tool for assessing advantages and disadvantages of the novel system. An analysis of the simulation results points out specific power system conditions under which operation of the all-digital system is most likely to fail. Manufacturers are expected to correct IEDs problematic performance in those situations before devices are made commercially available.
- The proposed methodology evaluates performance of the entire system. The UCA test subcommittee looks at performance evaluation of separate components.
- Compatibility and interoperability between IEDs from different vendors are demonstrated and tested by combining three different sensors and merging units with the same distance relay.

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Part II

Performance Evaluation of All-Digital Protection Systems

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1.0 Introduction

This report presents results of tasks, defined in the proposal for the project titled "Digital Protection System Using Optical Instrument Transformers and Digital Relays Interconnected by an IEC 61850-9-2 Digital Process Bus."

The tasks were:

1. Analysis of an all digital measurement and protection system operation using high voltage and high current.
2. Evaluation of American Electric Power Co. provided operation data and an overall comparison of the compatibility of the systems provided by different manufactures.

Tests were performed in Arizona State University's High Voltage Laboratory. A Synchronized High Voltage and High Current Generator simulated the fault-generated actual voltages and currents. The simulated high voltage and high current signals were analyzed in the optical supplied the optical instrument transformers and digital relays. Actual fault records from American Electric Power were analyzed, and signal wave shapes were used for fault regeneration.

This report presents the assessment of digital protection, the test scheme and its capability, test procedures, and test results.

The objective of this project was to investigate the feasibility of an all-digital protection system using optical instrument transformers directly interconnected through an IEC 61850-9.2 digital process bus with digital relays. The system operation was evaluated using computer simulation, laboratory measurement, and limited field tests [1].

2.0 Assessment of Digital Protection

2.1 Introduction

Digital protection systems consist of optical instrument transformers, a digital communication bus, and a digital relay. Optical instrument transformers measure the line voltage and current values and send the digitized measured values from its Merging Unit (MU) to a digital relay through a digital communication bus. Digital relay processes the digitized data by using different evaluation algorithms. Typical examples are: algorithm for over-current protection and algorithm for distance protection. According to the relay settings, the relay trips the circuit breaker or triggers an alarm signal.

This report presents:

- The development of a test facility for a digital protection system
- Regeneration of a typical power system fault by the facility
- The discovery of four different types of time inverse characteristics of digital relay
- An investigation of the effect of fault current with DC bias on relay tripping
- The capture of the digital process bus data compared with the relay disturbance records

2.2 The Digital Protection Concept

An electric power system uses a rapidly increasing number of digital systems. Power system protection is one of the main application areas of digital systems in the power industry. Optical voltage and current transformers, with digital output signals, supply the tested digital protection system, which contains a digital process bus and a digital relay. Figure 2-1 shows the typical arrangement of the instrument transformers, relay, and circuit breaker necessary for the protection of a power line.

This figure shows that the digital output signal of the optical voltage and current transformers is connected to the IEC 61850-9-2 process bus, which supplies a digital relay. The operator can record data through this bus on a laptop computer. The digital relay monitors the line operation and produces a tripping signal in case of fault. This signal initiates the circuit breaker and the clearing fault by switching off the faulty line. A computer in the control room monitors the relay operation.

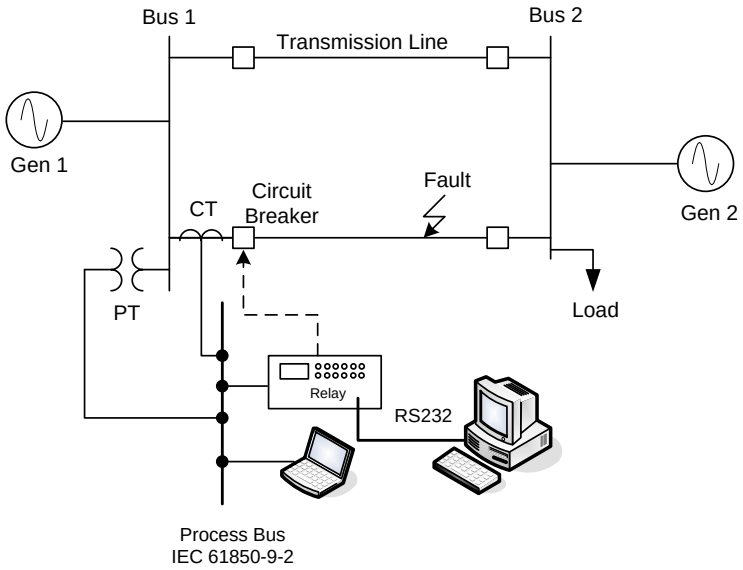


Figure 2-1. Power system protection physical model

Generally, distance relays protect transmission lines. One of the advantages of this method is that the relay identifies the fault location in addition to tripping the circuit breaker when there is a fault [2], [3]. The relay measures the voltage and current phasors and calculates the ratio of the voltage and current; this ratio is the impedance phasor [4]. When there is a fault, the impedance is proportional with the distance between the relay and the fault location. In general, changes in the phasors indicate load changes or the existence of a fault which needs to be cleared [5]. On the other hand, Microcontroller based relays provide reliability and accuracy. Accuracy of the current and voltage measurement (amplitudes and phase angles) is crucial for proper operation of the system. Magnetic current transformer saturation affects the calculation of line impedance and delays the relay tripping time [6]. The optical instrument transformers are not saturated.

Over-current protection is the other frequently used protection technique. With over-current protection, the relay trips when the line current exceeds the set value, which is frequently 1.5-2 times the rated current of the line. The efficiency of over-current protection can be improved by using relays with inverse time delayed characteristics. Figure shows the tripping time for a relay with inverse time delayed characteristics; the tripping time decreases when the current amplitude increases.

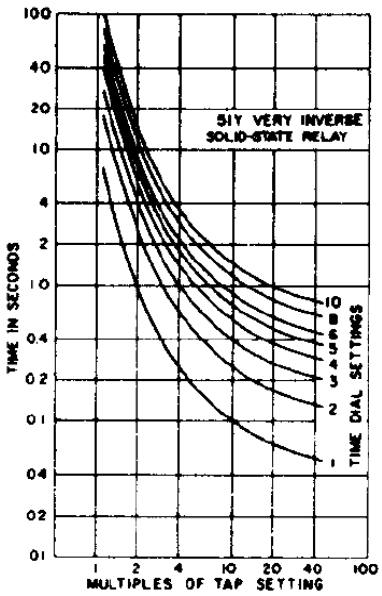


Figure 2-2. Relay tripping time [7]

Most digital relays can be adjusted to provide either over-current or distance protection. In this report, the operation of a digital relay is investigated when the relay is adjusted to provide inverse time over-current protection.

2.3 Fault Simulation

In order to test the digital protection system using optical instrument transformers interconnected by an IEC 61850-9-2 process bus, Arizona State University (ASU) has developed a dedicated test facility. This facility can be used for testing any type of protection systems [8], and it includes synchronized high voltage and high current generators to simulate real fault conditions.

The literature and actual fault records show that typically, a fault in a high voltage system causes a sudden increase in current and drop in voltage. These high voltage and high current signals are reduced by instrument transformers to measurable, low voltage/current values. The obtained signals supply the protection relay. The relay makes the trip decision by using these voltage and current sine waves from the instrument transformers.

In the laboratory, separately generated high voltage and current sine waves are applied to the instrument transformers to simulate the fault generated voltage and current in a transmission line. Both optical and traditional instrument transformers can be connected to the system at the same time, and the output of the transformers are connected to the digital and analog relays in order to observe the responses in simulated fault conditions.

The next chapter gives the description of the test setup for optical instrument transformers. This test setup generates synchronized high voltage and high current signals. However, tests have been performed only with optical current transformer due to the unavailability of protection equipments.

3.0 Test Setup Description

3.1 Introduction

Due to the difficulties of generating high voltage and high current at the same time in a laboratory, ASU developed a test facility that uses a separate high current generator and high voltage generator in order to simulate a power line fault in this facility. The local low voltage network supplies both of these generators. The concept of the system is shown in Figure 3-1. A high fault current (a few thousand amperes and DC offset/bias current) and high fault voltage (10kV to 69kV) are generated simultaneously and are supplied to the equipments under test. This facility allows testing of the equipments with a high current and high voltage, which simulates, in the laboratory, the field conditions.

Test system components are:

- A control circuit
- A voltage generator
- A current generator
    - A load current generator
    - A short circuit current generator

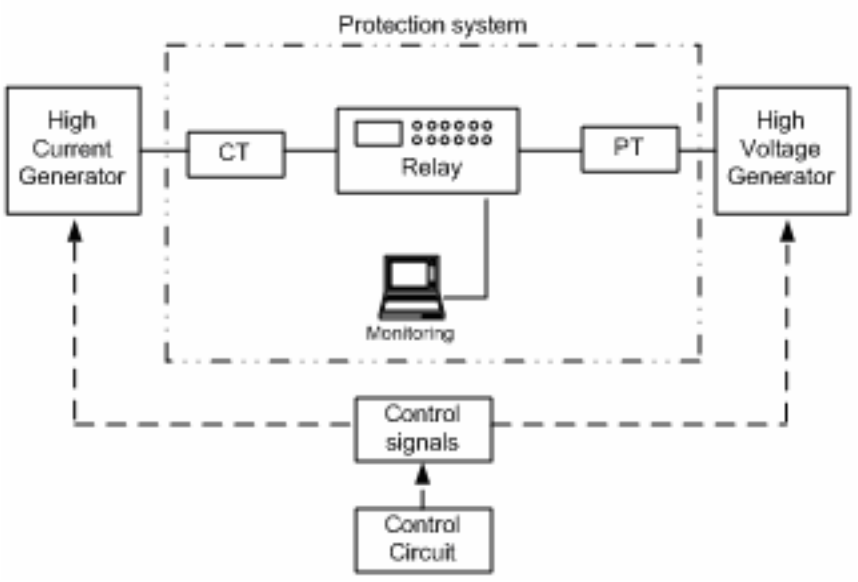


Figure 3-1. Test setup conceptions

A detailed circuit diagram of the system used for testing a system with optical instrument transformers is shown in Figure 3-2. A Current generator is on the left side of the figure in three different stages. A voltage generator is shown on the right side. The

control signals synchronize the operation of the two generators. A detailed description of each system components are given below.

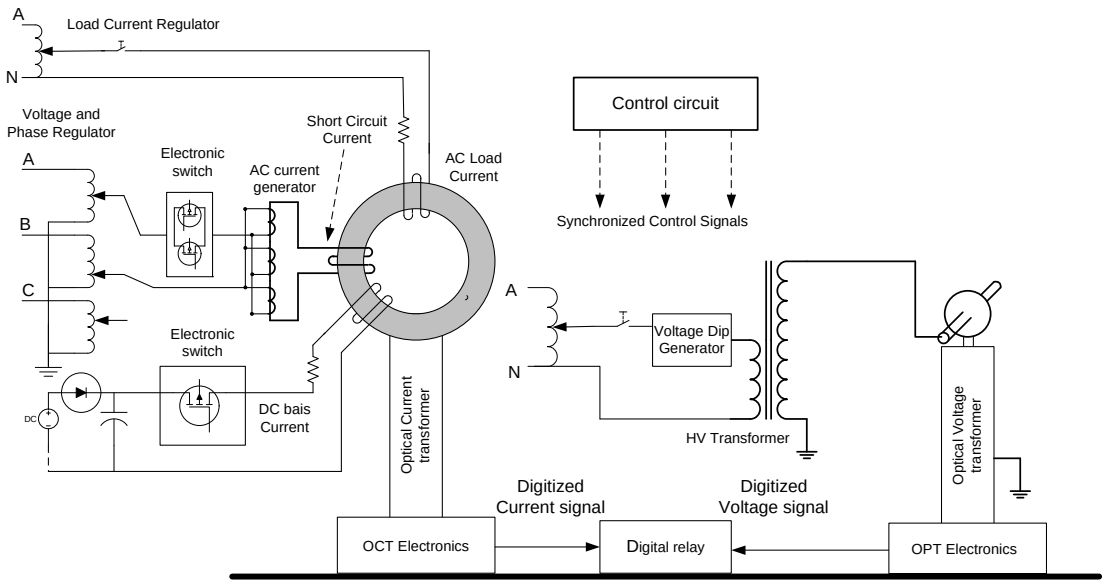


Figure 3-2. Circuit diagram for optical systems

3.2 Voltage Generator

A high voltage transformer supplied by the local low voltage network generates the test voltage, which supplies the optical voltage transformer. The pre-fault input to the high voltage transformer is controlled by a regulating transformer. The post-fault voltage magnitude is controlled by an adjustable voltage-dip generator. The timing of the voltage change is controlled by an electronic switch which is synchronized to the fault initiation. The simulation of the voltage sag during the fault condition is performed by a voltage sag generator (VSG). Figure 3-3 shows how the VSG is connected to the equipment under test (EUT).

The local low voltage line supplies a regulating auto transformer, which occurs before the fault supplies the rated nominal voltage for the high voltage transformer. When the fault is initiated, an electronic switch connects the high voltage transformer to the reduced voltage tap (sag voltage) of the auto transformer. This produces high voltage sag during the fault. The sag generation is synchronized to the network voltage and fault current generation. The “Signal shift circuit” permits the selection of the time on the sine wave when the sag is generated. The “Duration control circuit” regulates the sag duration.

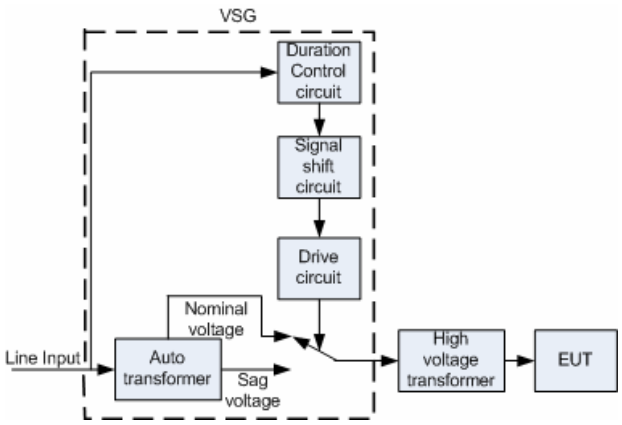


Figure 3-3. Voltage sag generator concept

The parts of the generator are:

The duration control circuit: this determines the duration of the nominal voltage and sag voltage, which can be changed from 2~60 cycles. A push button generates the starting signal (IS) for both the voltage sag generator VSG and the high current generator. The duration control circuit produces the end signal (ES), which terminates the process. The VSG generates a nominal voltage (pre-fault voltage) for 20 cycles, which is followed by the voltage sag for a variable duration; after the relay operation (fault clearing), the voltage is increased to the nominal value of 20 cycles. The duration of voltage sag can be selected from 2, 5, 10, 20, 30, 40, 50, and 60 cycles.

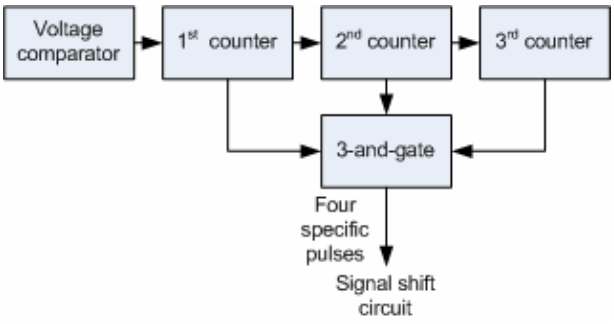


Figure 3-4. Duration control circuit

The concept of the duration control circuit is shown in Figure 3-4. One voltage comparator (LM311), three 10 decoded counters (CD4017) and 3-and-gates (7411) are used to regulate the duration of the nominal voltage and voltage sag.

The AC line voltage (110VAC) supplies LM311 through an isolation transformer (110/6 VAC), and LM311 converts the AC voltage (6 VAC) sine waveform to a synchronizing voltage square waveform, which has the same frequency as the input AC

source and a 0.5 duty ratio. This synchronizing square wave voltage is the clock signal for the first counter. The output signal (a duration of 10 cycles and a 0.5 duty ratio) of the first counter is the clock signal for the second counter. The output signal of the second counter (duration of 100 cycles and a 0.5 duty ratio) is the clock signal for the third counter.

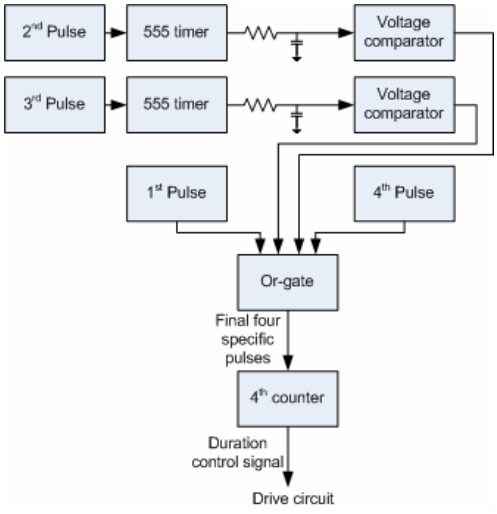


Figure 3-5. Signal shift circuit

By using three counters, any pulse between 2 and 1000 can be selected individually to control the operation. For example, if the 123rd pulse is needed, the 7411 chip is used to combine the 1st pulse output of the third counter, the 2nd pulse output of the second counter, and the 3rd pulse output of the first counter; then the output of 7411 will be the 123rd pulse. In order to get different sag durations (2, 5, 10, 20, 30, 40, 50, 60 cycles), the duration control circuit captures the 1st, 21st, 23rd, 26th, 43rd, 46th, 31st, 41st, 51st, 61st, 71st, 81st, 91st, and 101st pulses, and makes different combinations for the different sag durations. The square wave output signal of the duration control circuit supplies the shift circuit to regulate the sag beginning and ending points on the voltage wave. The 115th pulse is selected to be the ending (ES) signal. The three counters only count cycles during the time span from the starting (IS) pulse to ending pulse (ES). An eight (8) position DIP switch is used in a duration control circuit to select the voltage sag duration. Before the sag voltage is generated, the duration of the voltage sag must be chosen, and the related switch will be kept on, while other switches will be kept off.

The signal shift circuit: this is used to adjust the sag beginning and ending points on the voltage wave. The construction of the signal shift circuit is shown in Figure 3-5. The starting point of the sag/fault can be adjusted by delaying the duration control produced signals. The duration control produces two signals, the sag starting signal (2nd pulse) and sag ending signal (3rd pulse). The shifting or delaying of these two pulses can start or end the sag at any points on the voltage wave. The un-delayed or un-shifted 1st and 4th pulses determine the sag duration. Pulse 1 terminates the nominal voltage. The signal shift circuit can shift or delay the 2nd pulse and 3rd pulse up to 1 cycle. The delay/shift of the

2nd and 3rd pulses is realized by the following steps and Figure 3-6 shows the simulation's result:

- Either the 2nd or 3rd pulse (Figure 3-6 (a)) triggers a 555 timer, which generates a square wave signal with duration of 2 cycles' as shown in Figure 3-6 (b).
- The 2 cycles' duration square wave signal supplies a series connected RC circuit (10 kΩ; 1uF) as shown in Figure 3-6. The voltage across the capacitor increases gradually following a negative exponential curve. This gradually increasing voltage signal, shown in Figure 3-6 (c), is used to produce controllable delay.
- LM311 voltage comparator compares the gradually increasing voltage signal with an adjustable voltage (Figure 3-6 (c)) to get a delayed signal, as shown in Figure 3-6 (d). This delayed signal starts or stops the sag.

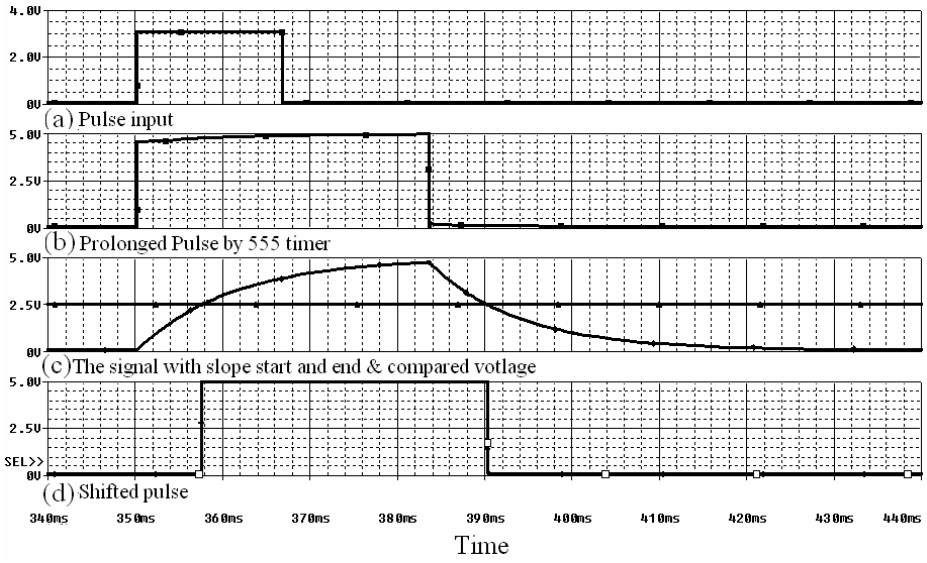
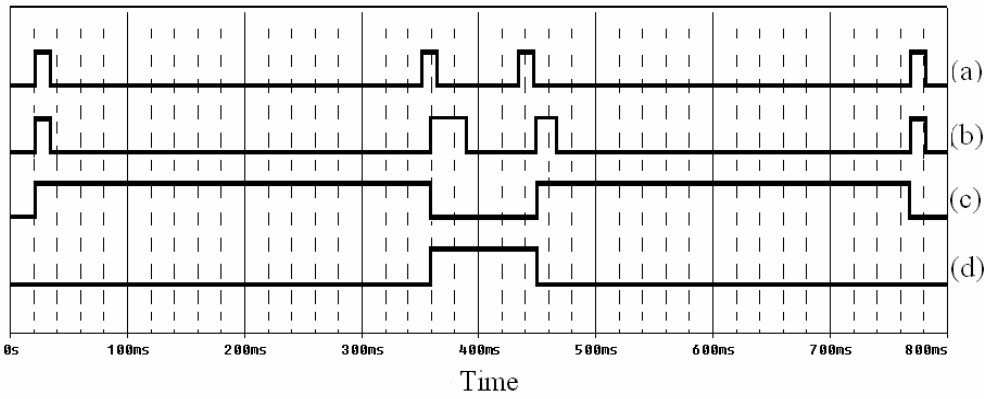


Figure 3-6. Pulse shifting

Figure 3-7 shows the corresponding simulation results for the VSG control signal with the shifted 5 cycles sag. In the below figure, the 2nd pulse is shifted a half cycle and the 3rd pulse is shifted one cycle. Figure 3-8 shows the simulated output voltage waveform. Figure 3-9 (a) and (b) show the control signals.

The drive circuit: this switches the high voltage transformer to the appropriate terminals of the regulating transformer to produce a nominal voltage and initiate voltage sag according to the control signal generated by the signal shift circuit. Two non-zero crossing solid state relays (SSRs) (one for the nominal voltage and one for voltage sag) are used to perform this operation. Figure 3-9 (c) shows the control signal that operates the SSR switch, which connects the high voltage transformer to the terminal that produces the nominal voltage. The duration in Figure 3-9 (c) is about 20 cycles. Figure 3-9 (d) shows the control signal that operates the SSR switch, which connects the high voltage transformer to the terminal that produces the sag voltage. The duration in

Figure 3-9 (d) is 5 cycles. The gate voltage turns on the solid state (SSR) switch. The removal of the gate signal switches off the SSR at the next current zero crossing.



a) The four special pulses supplied by the duration control circuit
b) The 2nd and 3rd pulses are shifted in the signal shift circuit
c) The control signal for nominal voltage at 5 cycles voltage sag
d) The control signal for voltage sag at a 5 cycles voltage sag

Figure 3-7. The input and output signals of the signal shift circuit

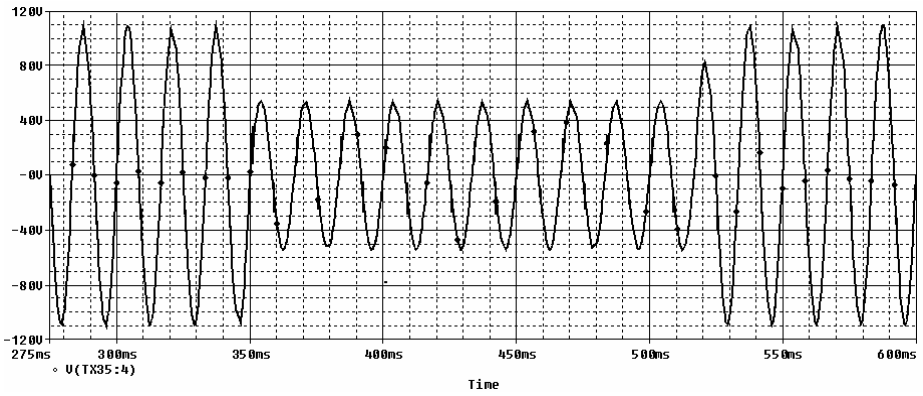


Figure 3-8. Generated voltage sag

The setting of the autotransformer and the nominal voltage of the high voltage transformer determine the magnitude of the nominal voltage and the voltage sag applied to the EUT. The solid-state switch characteristics must match with the regulating transformer and high voltage transformer's nominal voltage and load current. This requires changing the SSR when a different high voltage transformer is used.

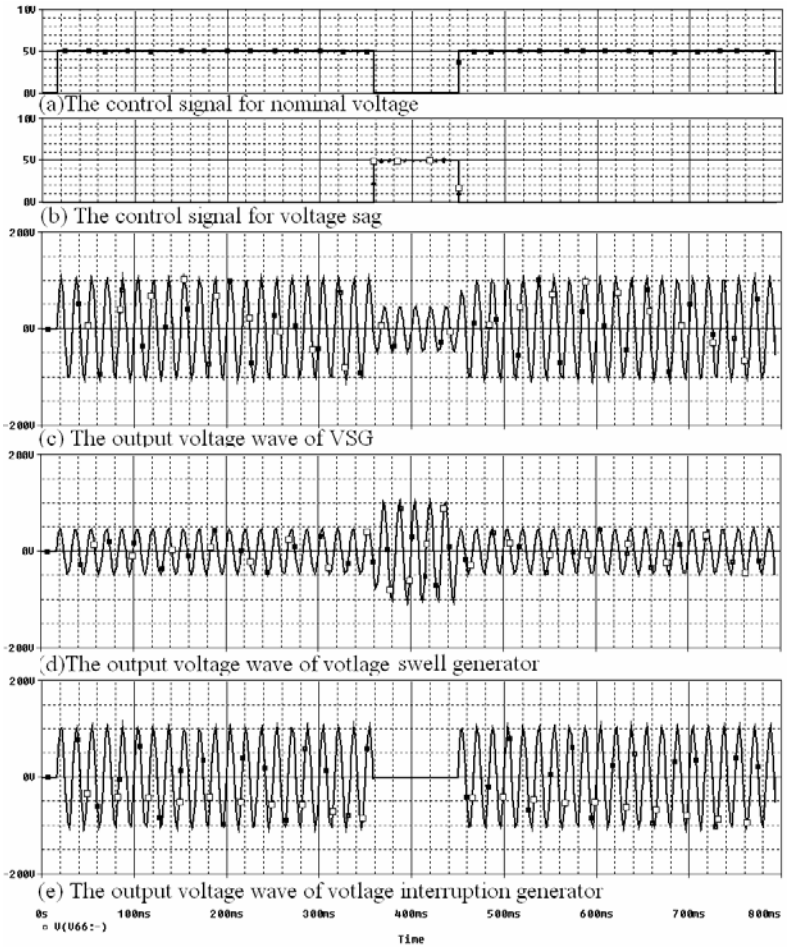


Figure 3-9. The output voltage wave of different VSG applications at a 5 cycles' sag duration

The single-phase autotransformer: this is used for generating two voltage levels: nominal voltage and voltage sag. The line voltage and the adjusted autotransformer outputs are applied to the primary side of the high voltage transformer.

The single-phase autotransformer provides two voltages (nominal voltage and sag voltage) to electronic circuits. VSG acts as a voltage swell generator, as shown in Figure 3-9 (d), if the terminals are interchanged. VSG can be used as a voltage interruption generator or circuit breaker, as shown in Figure 3-9 (e), if the sag voltage source is not connected to the electronic circuit. The single-phase autotransformer also can be replaced by two single-phase transformers in order to obtain a special nominal voltage and voltage sag.

Figure 3-10 shows the control circuit of the voltage sag generator. Figure 3-11 shows the general arrangement of the test circuit. The specifications of the high voltage transformer used in this set up are:

- Voltage 69 kV, BIL 350 kV
- Pri Volts/ Sec Volts 40250 V / 115 V
- Thermal Rating 6000 VA

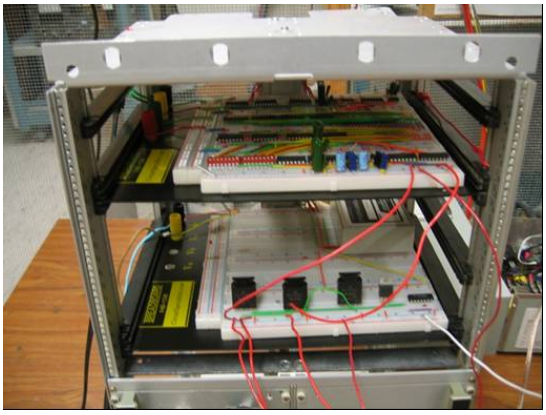


Figure 3-10. Voltage Sag Generator control circuit

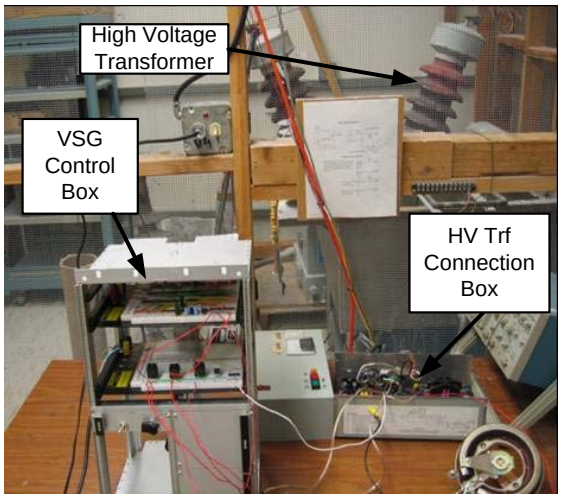


Figure 3-11. VSG connected to the high voltage transformer

3.3 Current Generator

The load current generator: the local 120V network, through a regulating transformer, supplies the secondary 5A windings of two 800/5 A ring type current transformers connected in parallel. An insulated conductor is passing through the ring of the current transformers to generate the load current. A regulating transformer controls the magnitude of the load current, between 0-60A. The conductor carries the load current thread through the optical current transformer ring. Using 10 to 30 turns, a load current of 200 to 600 amps can be simulated.

The short circuit current generation: Figure 3-12 shows the circuit diagram for short circuit current generator. Three ring types of 600/5 amp current transformers generate the fault current. The 5 amp secondary winding of the current transformers are connected in parallel and supplied by a three phase regulating transformer. The regulating transformer controls the amplitude of the short circuit current.

The electronic switch permits the selection of the fault initiation time. The short circuit can be initiated at any time between zero and 180 degrees on the source voltage wave. The maximum allowable current in the primary circuit is 1200 amps.

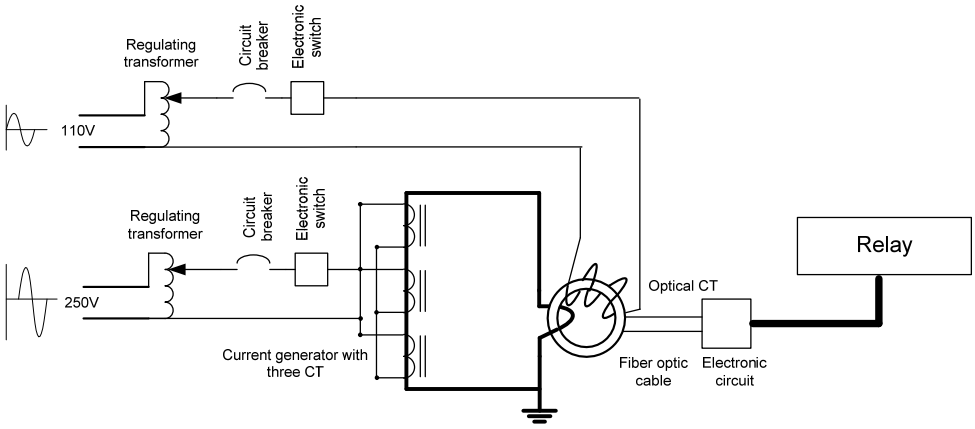


Figure 3-12. The short circuit current simulation test setup

The phase angle between the generated sag voltage and the short circuit current during the fault is controlled by supplying the regulating transformer from the line-to-line voltage of phase AB, BC, or CA. As an example, the change for AB to BC produces a 120-degree phase shift. Changing the amplitude of the supplied line-to-line voltage not only changes the generated current amplitude but also changes the phase angle of the generated current. This method allows for generating the short circuit current with various phase differences compared to the sag voltage phase during the fault, like 90 degrees.

DC offset generation: A DC component of the fault current can be simulated by the use of the DC bias current circuit, which discharges a charged capacitor through a few turns on the optical current transformer. The electronic switch, which discharges the capacitor, is synchronized with the initiation of the short circuit current and sag generation. The total current that the OCT measures is the sum of the short circuit current and the DC discharged current. The magnitude of the DC offset is controlled by varying the voltage of the capacitor's DC power charging supply. The decay rate of the DC component can be controlled by varying the circuit parameters in the DC bias current circuit. Figure 3-13 shows the DC offset generation circuit model, and Figure 3-14 shows the photo of the capacitor discharge circuit, which generates the DC bias current.

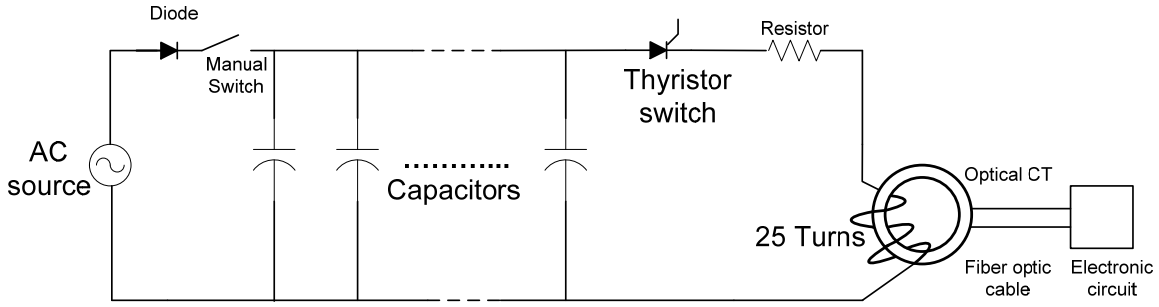


Figure 3-13. DC offset generation circuit model

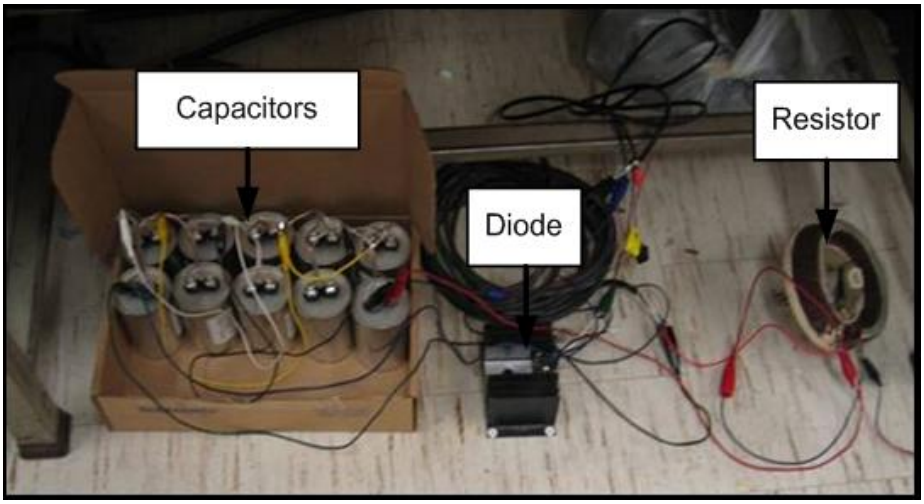


Figure 3-14. DC offset generation circuit

The line voltage is represented by the applied high voltage (around 69kV), and the line current is represented by the current generated by the load current generator (around 300A) during pre-fault. When the fault is simulated, control signals are sent

simultaneously to the voltage generator to create sag, to the current generator to produce the short circuit current, and to the DC bias current generator to enhance the DC bias current. Electronic switches are used to generate the load current, initiate the fault, and switch off the circuit after each test. The operator selects the fault duration, but after the fault, the system returns to the pre-fault condition. The phase shift between the current and voltage is adjusted by using different combinations of line-to-line voltages to generate the short circuit current. This allows for making different phase shifts, and, as a result, it allows for simulating different fault locations.

3.4 Test Results

This test setup was installed at A.S.U.'s High Voltage Laboratory. In order to investigate the test setup performance, an optical current transformer and an optical voltage transformer were supplied by the current and voltage generated in the test setup.

Figure 3-15 shows the recorded analogue output of the instrument transformers in the case of a typical three phase fault. The phase difference between the load current and line voltage is due to the inductance of the current generator. The phase difference between the short circuit current and sag voltage is, as expected, almost 90 degrees. Short circuit current switching has a slight delay, as shown in Figure 3-15. The quickly attenuating DC offset of the short circuit current is high enough to simulate the transients.

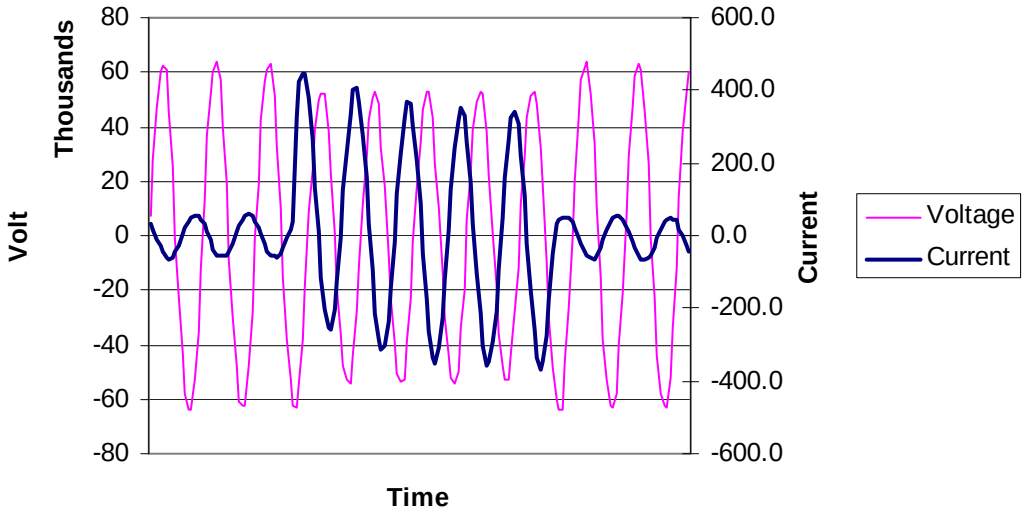


Figure 3-15. Short circuit simulation for five cycle

Several tests were performed using different test parameters. Figure 3-16 shows different switching points of the sine wave, which affect the DC offset voltage. Figure 3-17 shows a two-cycle fault simulation.

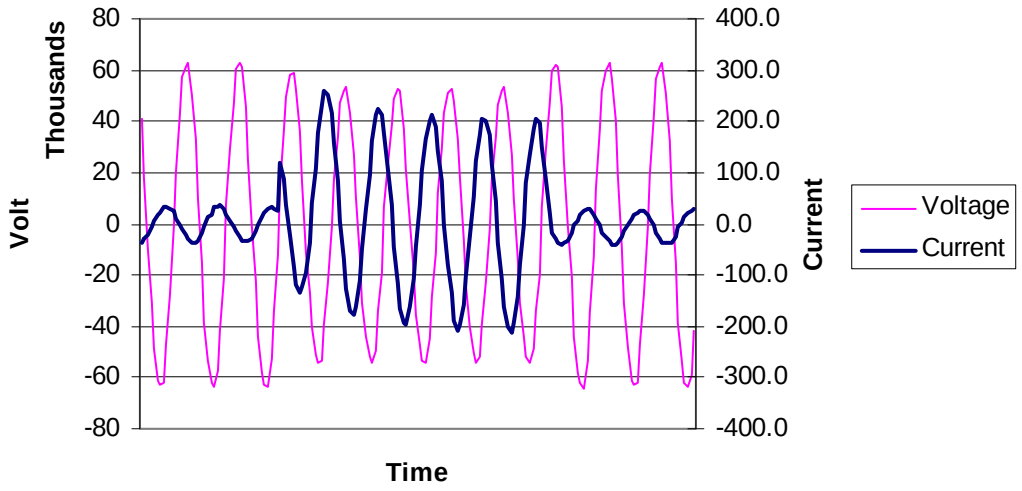


Figure 3-16. Short circuit simulation for five cycle non-zero switching

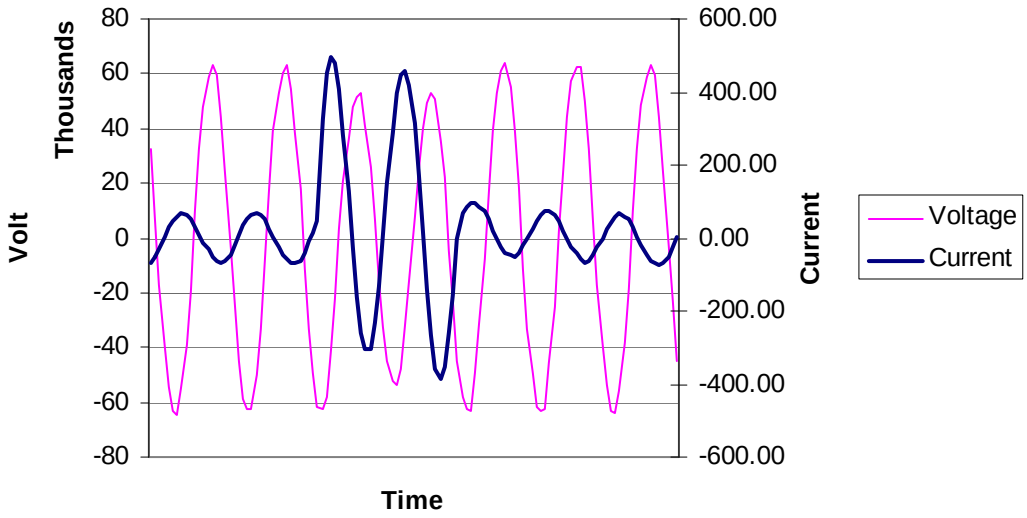


Figure 3-17. Two cycle fault simulation

These tests proved that all of the important parameters of the short circuit current and voltage during the fault are adjustable within a practical range. Consequently, it was concluded that the dedicated test facility was suitable for simulation of transmission line faults.

4.0 Digital Protection Test Setup and Procedures

4.1 Introduction

This section presents the experimental study of a digital protection system performed in the dedicated test facility described in the previous section. Due to the lack of equipments, experiments were performed using only the NxtPhase Optical Current Transformer and AREVA Digital Relay.

The first part of this section describes the test setup and the settings for the relay. The second part describes the test of an AREVA Digital Relay in over-current protection mode. Finally, the digital process bus communication records were compared with the digital relay provided records.

4.2 Test Setup

Figure 4-1 shows the one line diagram used to test the all digital over-current protection. The major components are:

- The current generator of the test set up
- NxtPhase optical current transformer (OCT), with Merging Unit (MU)
- AREVA digital relay
- A computer

The current generator of the test facility supplied the NxtPhase optical current transformer (OCT) with different over-currents. The digital output of the OCT Merging Unit was connected to the digital communication bus, which supplied both the AREVA digital relay and a computer. The computer recorded the data sent to the digital relay. The short circuit current carrying conductor was turned twice on the OCT sensor head to increase the applied current. The maximum applied current became 2200 A. Figure 4-2 shows the picture of the testing of the AREVA relay.

The specifications of the different devices were:

NxtPhase NXCT-138 Optical Current Transformer:

- Max System Voltage: 145 kV
- BIL: 650 kV
- One minute withstand voltage (wet): 275 kV
- Rated frequency: 60 Hz
- Weight: 152 lbs
- Rated max thermal current: 3000 A

- Rated Short-circuit current : 63 kA
- 1C Accuracy (relaying): n/a
- 2C Accuracy (metering): 0.15

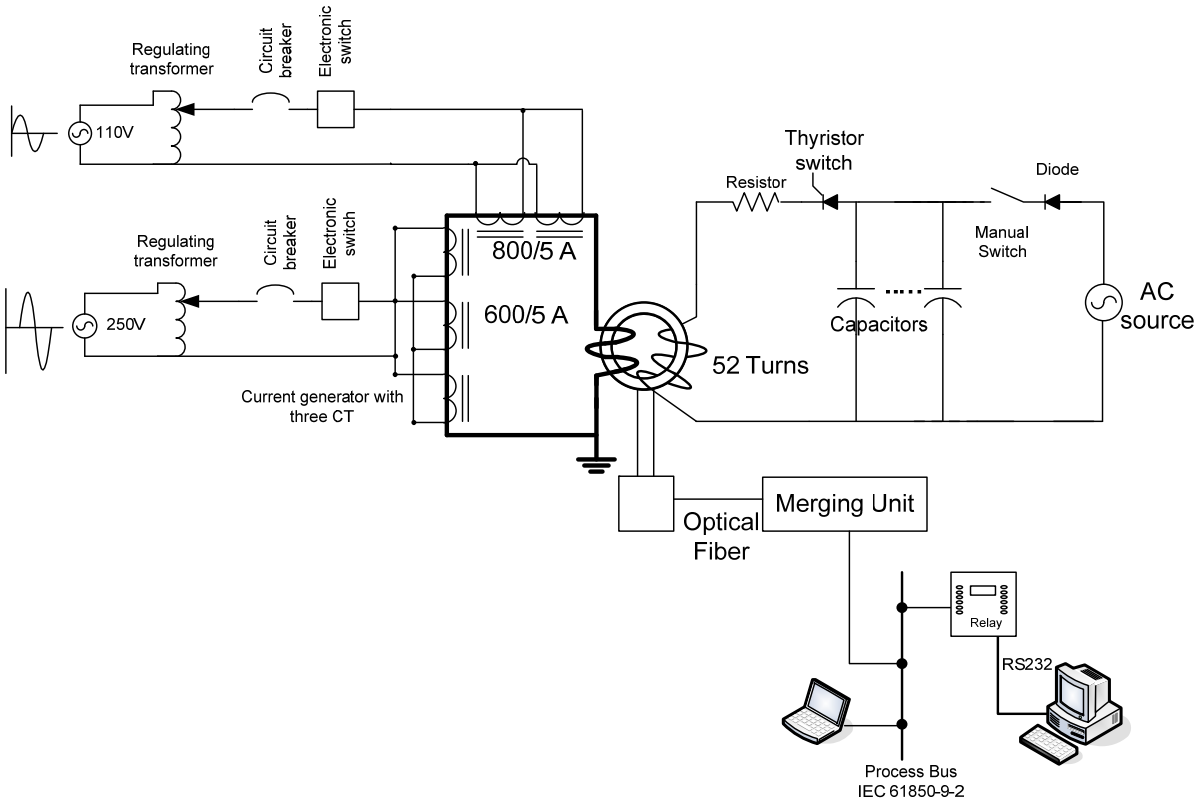


Figure 4-1. The test setup for the all digital over-current protection

AREVA Micom P440 relay:

- Nominal voltage: 24-125 VDC /110-250 VAC
- Operate range: 19-300 DC / 24-265 VAC
- Digital inputs: (Vmin/Vmax Tresholds) 24/27, 30/34, 48/54, 110/125, 220/250
- Output contacts: max 46
- Setting groups: 4(2)
- Fault records: 5
- Event records: 250-512
- Disturbance record: 75 s max
- IEC 61850: Yes

Fluke 189 True RMS multimeter was used to measure the output voltage of the transformers and the capacitor voltage. Specifications of this multimeter are given below:

- Model: 189
- Voltage range: 2.5 mV to 1000 V- 100 kHz bandwidth
- Frequency: 0.5 Hz to 1000 kHz
- Accuracy (Basic DC V): 0.0025%, (Basic AC V): 0.4%

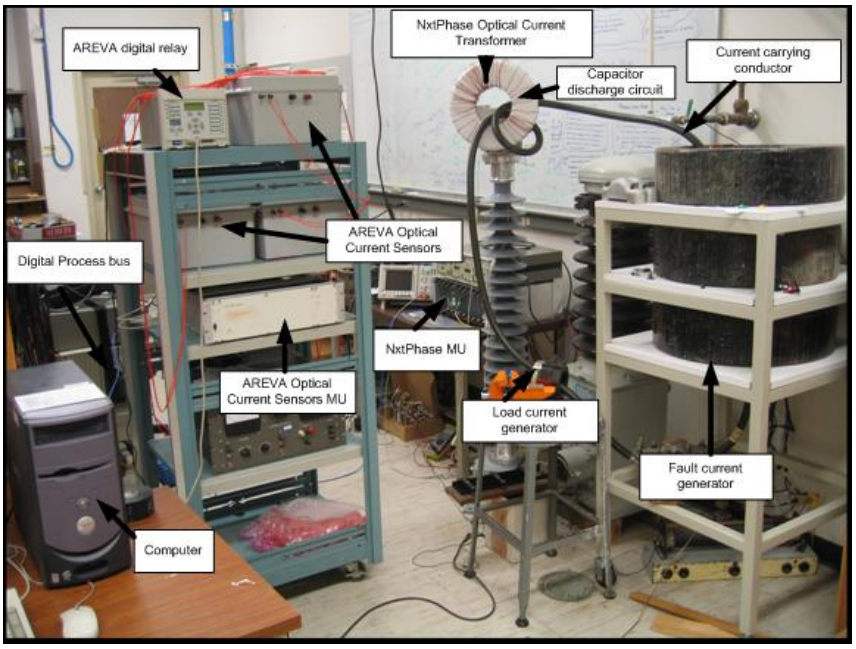


Figure 4-2. Picture of the test setup for the all digital over-current protection

The following tests were performed to verify the proper operation of an all digital protection system. The test procedure was:

- The digital relay was set to the inverse over-current protection mode by selecting an inverse time delayed characteristic and threshold current.
- The relay was set to a high threshold current to prevent tripping.
- The high current generator, together with the DC offset current generator, was activated to produce a fault current.
- The relay recorded the fault current but did not trip because of the high threshold setting. The relay record was reviewed to verify that the fault current was the desired test value.
- The relay threshold current was adjusted to the selected value.
- The DC bias capacitors were re-charged to provide the DC offset current, and the high current generator was reactivated to produce the fault current again.
- The laptop connected to the processing bus recorded the fault current using a network analyzer program.
- The fault current activated the relay, which produced an alarm signal or even a tripping signal.
- The Circuit switched off, and the disturbances records were downloaded from the relay.
- Results were analyzed.

4.2.1 Digital relay settings, ratio settings

The AREVA Micom P440 relay has different features, which can be adjusted to the desired functions. This relay can operate both as a distance relay and as an over-current relay. In over-current mode it can operate as a directional over-current relay without time delay, with definite time delay, or with inverse time delay. Because of not having an optical voltage transformer with digital output, the failure of the voltage divider of the AREVA Merging Unit, and the failure of the AREVA MU digital output, the relay in distance protection or directional over-current mode was not tested. The tests were limited to the investigation of relay operation in non-directional over-current mode with definite time delay or with inverse time delay. The relay has four different inverse time delayed characteristics, which are:

- IEC E Inverse Curves
- IEC S Inverse Curves
- IEC V Inverse Curves
- IEEE V Inverse Curves

The AREVA relay has four over-current elements. The first two elements, with adjustable threshold currents of I1 and I2, can operate with definite time delay, with inverse time delay, or without time delay. The two other elements, with threshold currents of I3 and I4, can operate only in instantaneous or definite time delayed tripping mode.

According to the relay specifications [9], the relay in inverse time delayed mode calculates the time delay by the following formula:

$$t = T \times \left(\frac{K}{(I / Is)^{\propto} - 1} + L \right) \qquad (1)$$

Where:

t = operation time
K = constant
I = measured current
Is = current threshold setting
α = constant
L = ANSI/IEEE constant (zero for IEC)
T = time multiplier setting

Figure 4-3 shows the typical calculated very inverse delay time characteristics of the relay. The operation time of the relay depends on the fault current. The figure shows that larger fault currents results in faster operation.

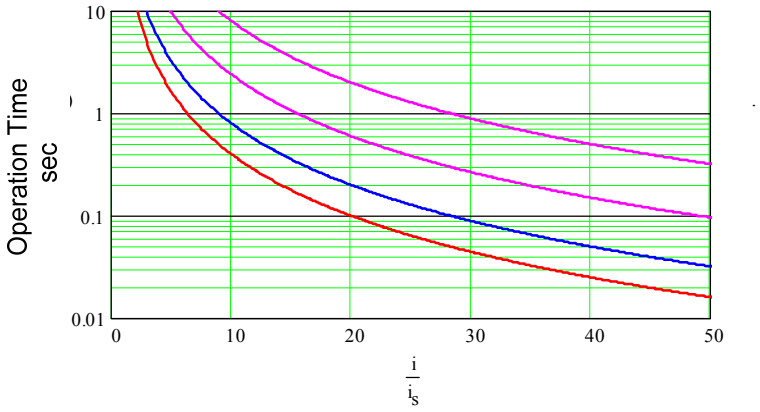


Figure 4-3. Typical calculated very inverse time delayed characteristics

In general if the fault or primary current is less than the threshold current, the relay output is zero. When the fault current exceeds the threshold current, the relay produces an alarm signal and calculates the required delay time using equation 1 or adjusting the delay time according to the required definite time delay. After the delay time, the relay produces a trip signal if the fault current is on. If the fault is cleared by another relay before the delay time is over, the relay will not operate; it will be reset automatically.

Since the OCT and the relay are from different manufacturers, there was a current transformer ratio mismatch in the relay settings. This mismatch was experimentally corrected using a magnetic current transformer and the relay reading.

During the test of the protection circuit, the applied current amplitude was varied, and the relay response was evaluated by analyzing the disturbance records. The threshold current was adjusted to 100A. The maximum peak current was 2200A, which corresponded to 22 times the threshold current.

4.3 Over-current Protection Tests

4.3.1 Short circuit simulation

The relay was set to the over-current protection mode using the IEC E inverse characteristics with a 100 A thresholds or pick up current because any value above 100 A trips the relay, which produces an alarm signal. Figure 4-4 shows the relay operation when the fault current was only 101 A rms with a high DC bias current. The instantaneous value of the fault current was above 100 A, and as a result the relay gave an alarm signal and calculated the delay time, which was significantly more than 60 cycles because of the inverse time delayed characteristics. The figure shows that this current was switched off by the high current generator after 60 cycles; consequently, the relay did not produce a trip signal. However, the relay recorded the disturbance as shown in Figure 4-4. The record includes the current signal and trip signal. The figure shows only the current signal but not the trip signal.

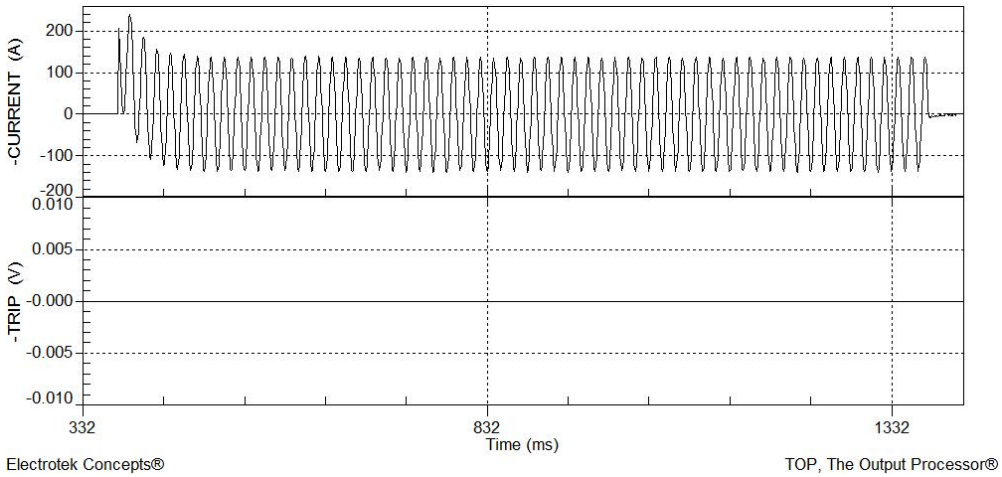


Figure 4-4. 100 A continuous current

The test was repeated using the same current; however, the current was not switched off after 60 cycles but maintained for about 10.5 seconds. Figure 4-5 shows that the relay produced a square shape tripping signal after about 10.1 seconds. Figure 4.4 shows that the fault duration was 10540 ms and the tripping signal length was 1687. This made the tripping time around 10540-1687=8853 ms =8.8s. The time scale of Figure 4-5 is compressed because of the long duration of the fault. Figure 4-6 shows the end part of the same record in more detail.

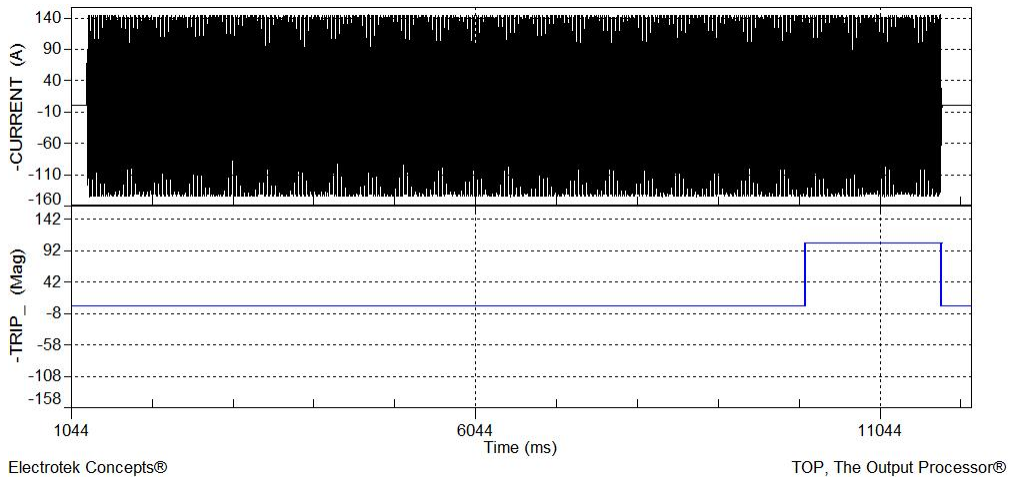


Figure 4-5. 100 A continuous fault

Figure 4-6 shows the ending period of the same fault record. The relay tripped after 8.853 sec of the fault initiation and kept the contacts on until the fault current terminated. It was expected that the contacts would stay on even after the fault cleared when the fault current went to zero. After tripping, the relay requires manual resetting.

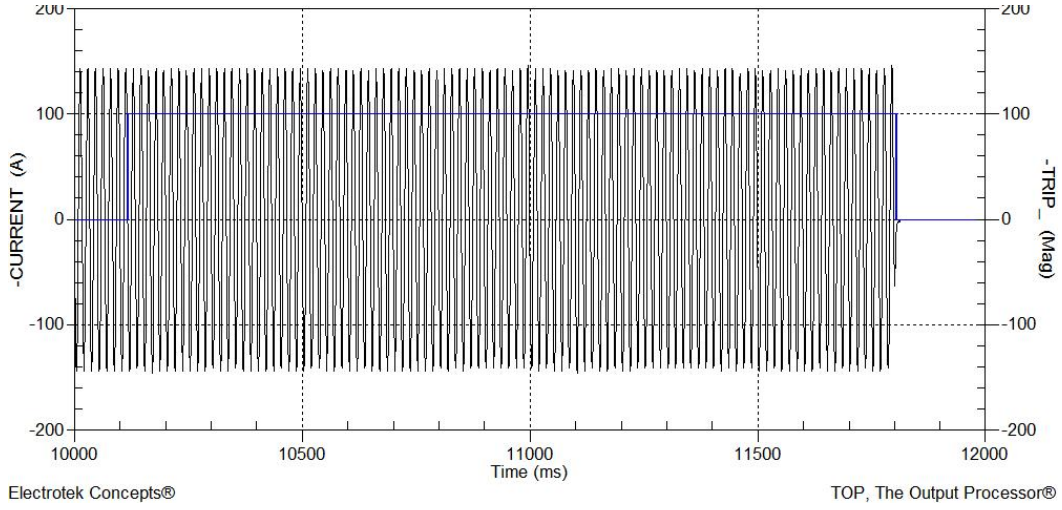


Figure 4-6. 100 A fault ending

The applied fault current was increased to 500 A rms. It was applied for 60 cycles in order to trip the relay. The relay tripped at 95.7 ms after fault initiation, which was much shorter than the 100 A fault tripping time. Figure 4-7 shows the relay record of the fault current and the square shape of the tripping signal. The figure shows that the relay tripped after around the 6th cycle of the fault, and it ended when the fault current became zero. This was the same as with the 100 A tripping.

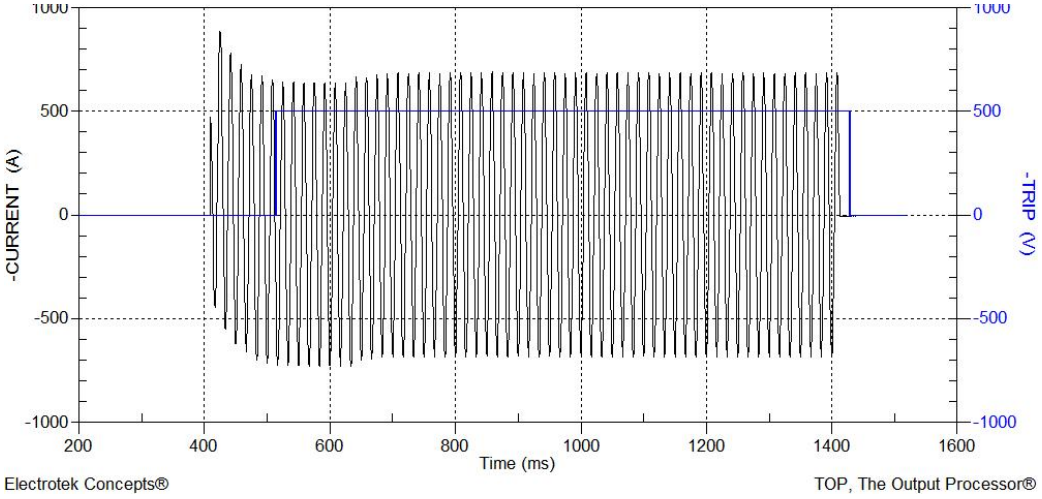


Figure 4-7. 500 A fault simulation

The applied fault current was increase to 2200 A rms, which is 22 times the threshold current value of 100 A. The relay tripped in a very short time after the fault initiated. It tripped after 15.4 ms and in the first cycle of the fault.

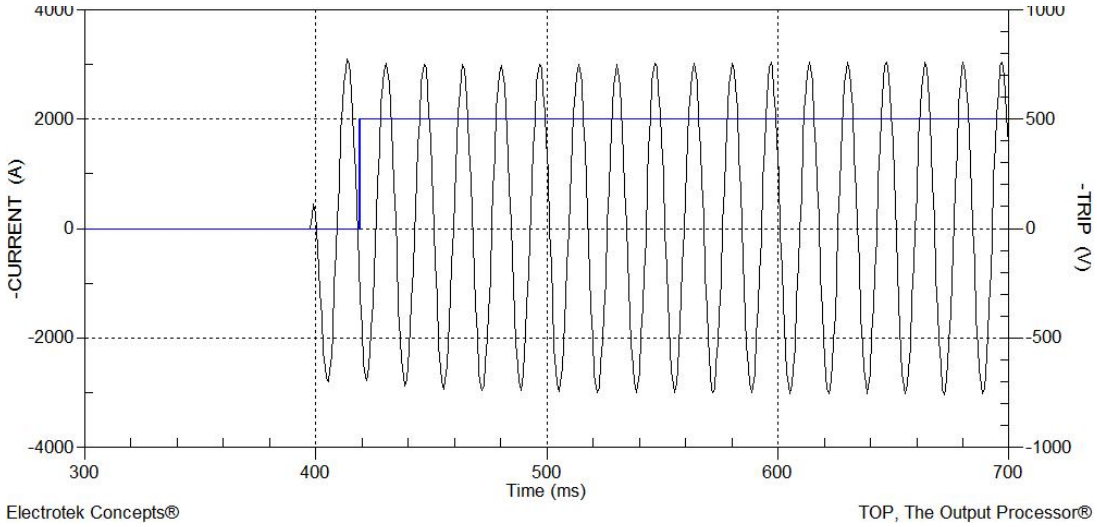


Figure 4-8. 2200 A fault simulation

The same methodology and steps described above was repeated for the four time inverse characteristics. For each characteristic, the relay tripping time was recorded in three ways: calculating the tripping time by using the computer recorded data sine waves, using the information about the fault on the relay LCD, and calculating the tripping time with the equation given in (1). Three calculated curves were plotted together to show the four characteristics, this is shown in Figure 4-9, Figure 4-10, Figure 4-11, and Figure 4-

12. Calculation of the tripping time from the recorded sine wave was almost identical to the relay reading values. However, the calculation of the tripping time by using the equation (1) was significantly different than the other two curves.

The below figures show that in the IEC curves the calculated and the recorded readings match; however, in the IEEE curve the calculated values do not match the relay readings and records.

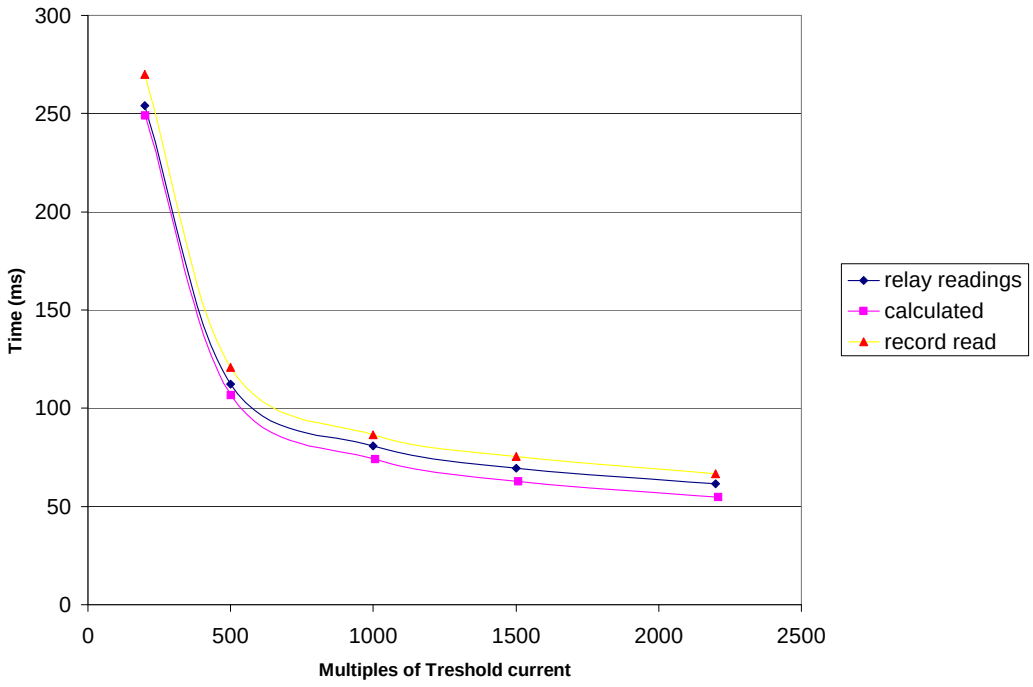


Figure 4-9. IEC S inverse characteristic

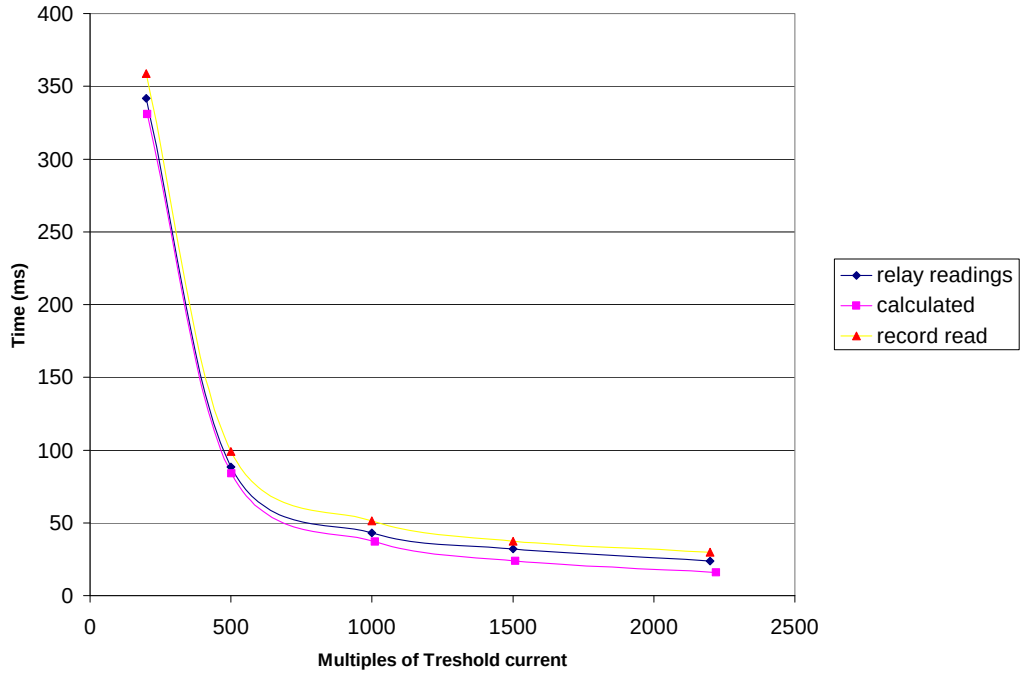


Figure 4-10. IEC V inverse characteristic

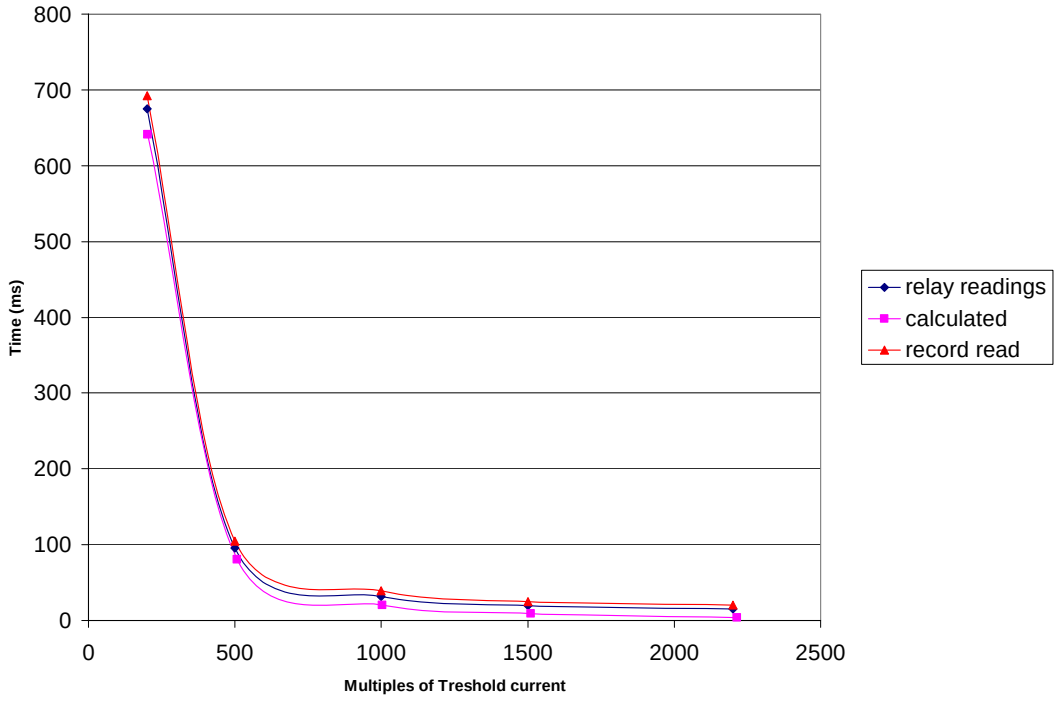


Figure 4-11. IEC E inverse characteristic

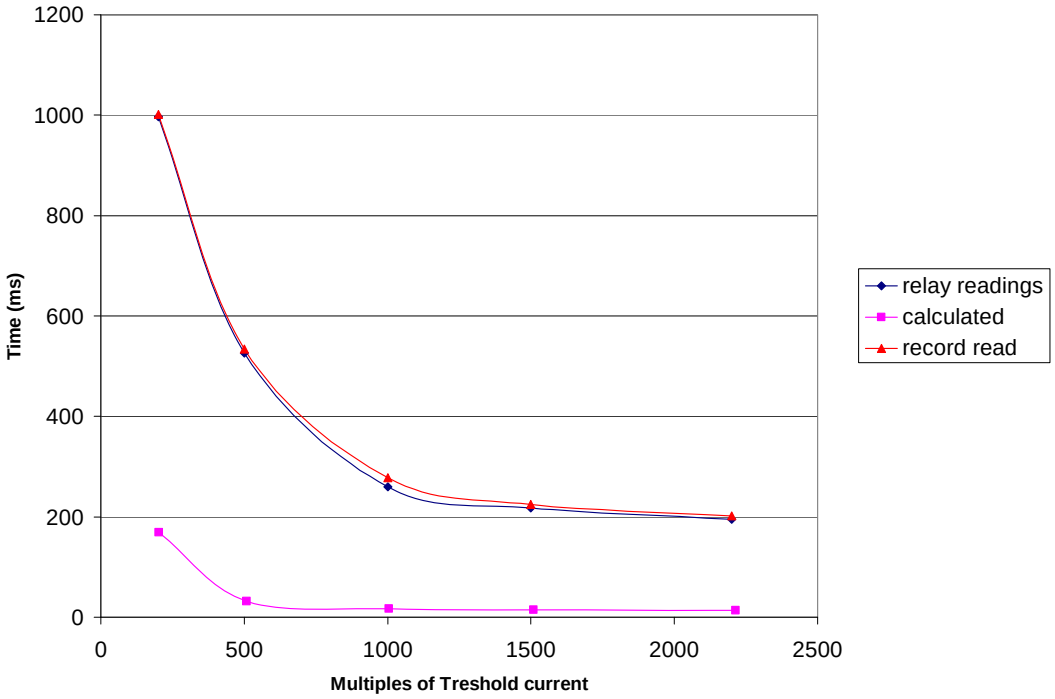


Figure 4-12. IEEE V Inverse characteristic

4.3.2 DC bias effect on trip/alarm

When a fault occurs in a power system, a DC offset will appear due to the inductance and resistance of the system components. The effect of the DC offset was investigated earlier in [10]. Figure 4-13 shows a typical DC offset's affect on a current sine wave.

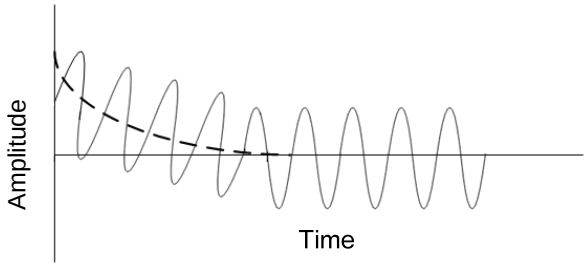
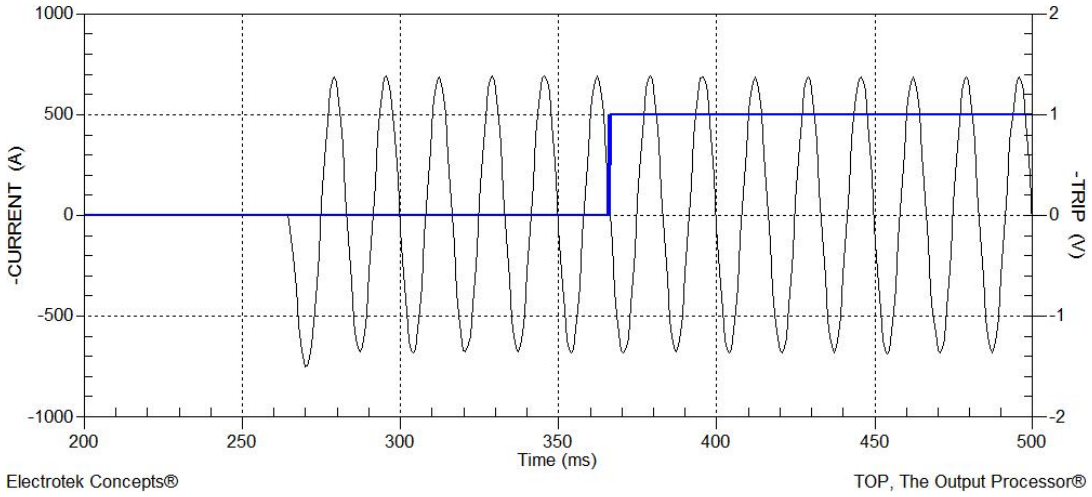


Figure 4-13. Fault current with DC bias

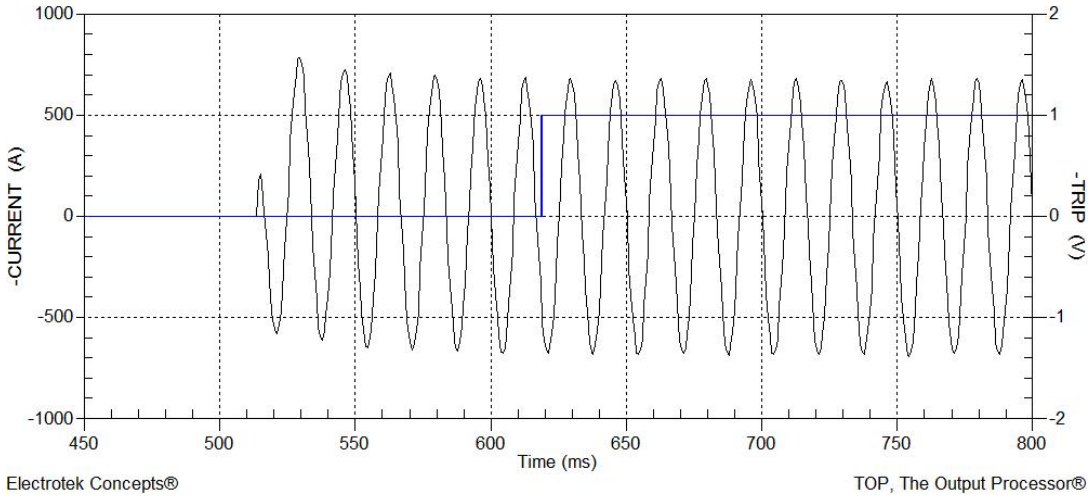
Figure 4-13 shows that for the first few cycles, the current value increases, but after the DC component attenuates, the current becomes constant. In order to find the DC offset's affect on tripping, three different values of DC bias levels were applied to the

relay along with a 500 A rms fault current. The fault current and relay tripping times were plotted in the same below figures after the tripping times were calculated.

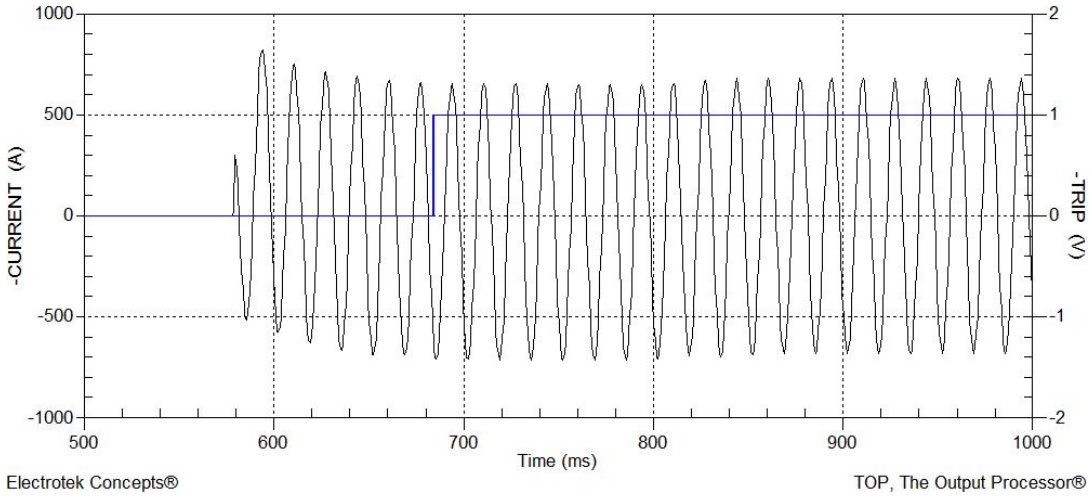
Figure 4-14 a), b), c), and d) show the recorded data of a consistent fault current with different DC offset currents. The recorded and analyzed results show that the relay tripping was almost the same for 0%, 10%, 15%, and 25% of the DC offset current. The relay tripped after the 6th cycle in each case.



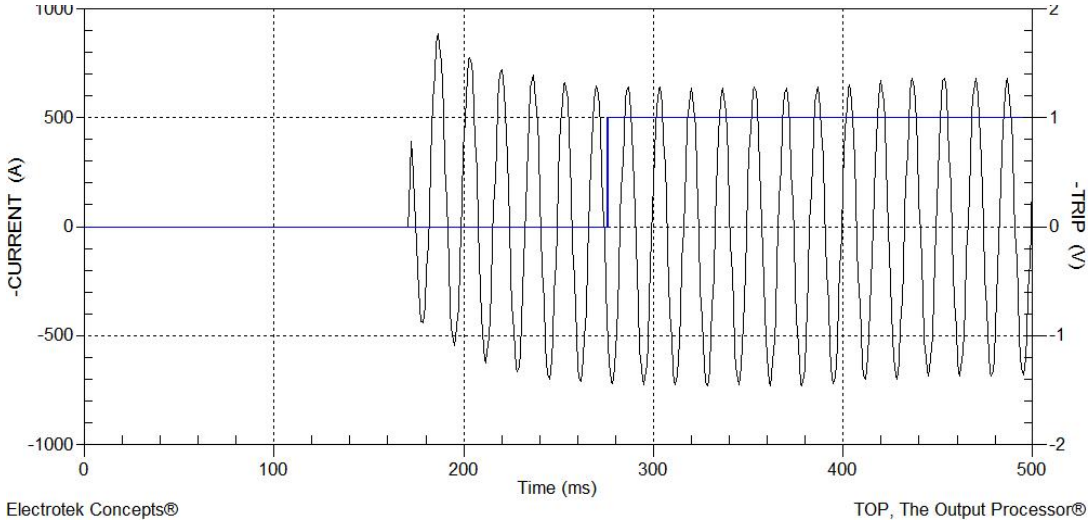
a)



b)



c)



d)

Figure 4-14. DC Offset effect

4.3.3 The effect of the impulse current on the trip/alarm

Switching transients frequently produces an impulse type transient current superimposed on the small AC load current. An impulse current was generated by discharging the capacitor used for the DC offset current generation, and the effect of this

impulse current on relay operation was investigated. Figure 4-15 shows the applied impulse current and the tripping signal.

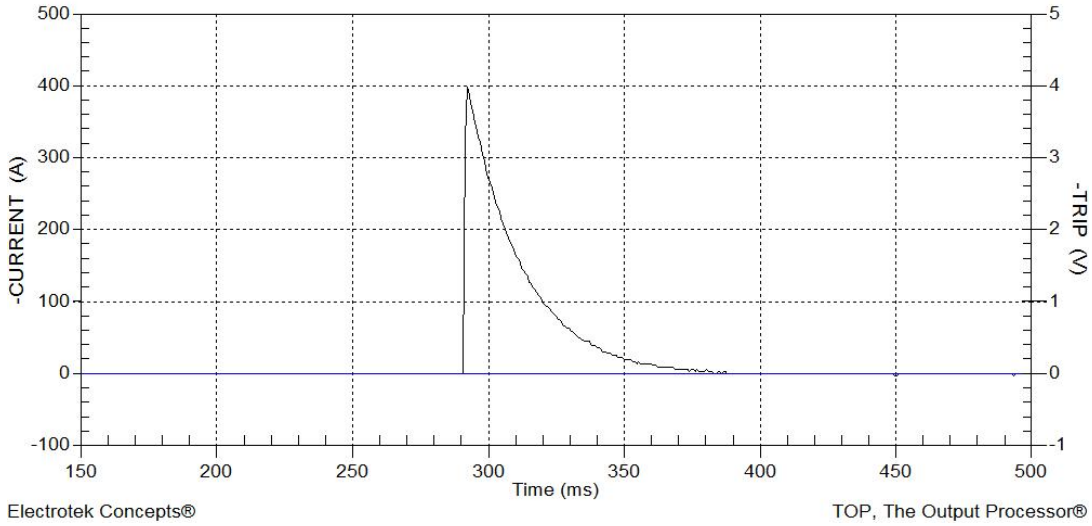


Figure 4-15. The impulse current test

The experimental results showed that the digital relay gave an alarm signal if the impulse current was above the threshold value. The applied maximum impulse current was 400 A, which was above the threshold current, and its duration was 100 msec. Figure 4-15 shows that the relay did not trip and gave only an alarm signal.

This is an important result because the relatively short duration switching surge is not a fault, so it should not trip the relay.

4.3.4 The load current and short circuit current simulation

All the experiments were performed without a load current; to verify that the load current did not effect the relay operation, tests were performed using a 60A load current and a fault current of 700A with DC offset. The relay was set to 100 A of the threshold current. The experiment was conducted by using the test setup described in section 3.3. Because the fault current was over the threshold value, the relay gave an alarm, and after delay, generated a trip signal.

The disturbance recorded by the relay was downloaded; it is shown in Figure 4-16. This figure shows the recorded sine wave current and relay tripping decision. The relay tripped according to the characteristics described in the previous sections. The test demonstrated that the load current had no effect on the relay operation if it was less than the threshold value.

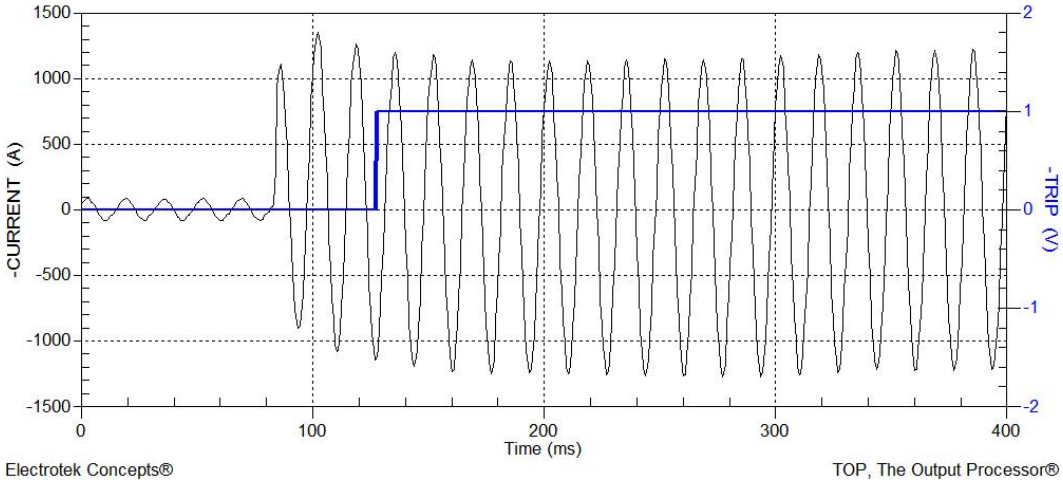


Figure 4-16. Actual fault simulation

4.4 The Digital Process Bus and Records

The communication between the relay and merging unit was trough the 61850-9-2 digital process bus. The current readings from the optical sensor head were processed and digitized by the merging unit and sent to the relay through the process bus. This data was captured by the AREVA 61850 network analyzer program, which was installed on a personal computer. Using this program, digitized data was captured for a long time period and saved on the computer. Fault simulation was performed, and the fault data was recorded with the network analyzer program and was compared with the relay disturbance records. Because the program and the optical sensor were different brands, there was a scaling (ratio) problem similar to that identified at the relay. A scaling factor was experimentally determined because it was recognized that the sine waves were close to identical. Figure 4-17 shows 500 A fault disturbances. The figure shows that the amplitude of the current, captured by the computer at the process bus, is too high and does not match the relay values. This data must be divided by 50 to match the relay captured values shown in Figure 4-17.

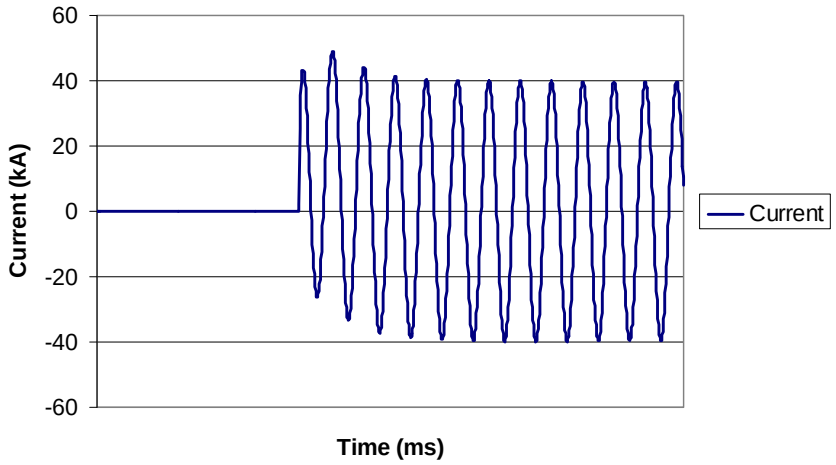


Figure 4-17. Data captured from the digital process bus

Figure 4-17 and Figure 4-18 show the actual fault simulation and impulse current recordings. The same problem of amplitude value is still seen. However, the wave shapes of the signals do match the signals of Figure 4-15 and Figure 4-16.

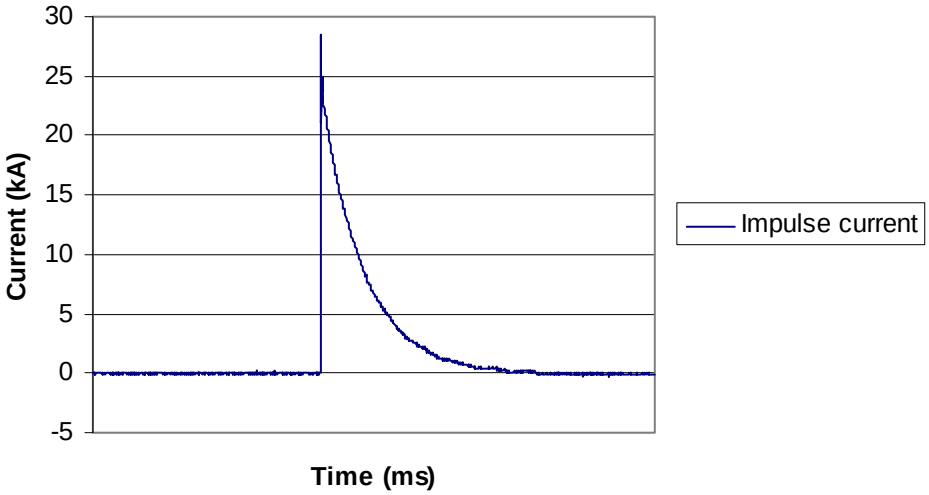


Figure 4-18. The process bus data for the impulse test

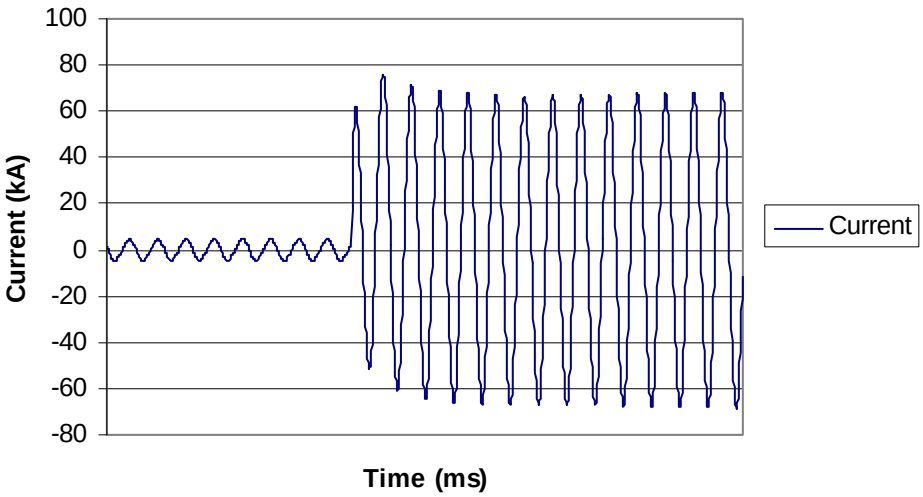


Figure 4-19. The process bus data for the actual fault simulation

5.0 Conclusions

In conclusion, the all digital over-current protection operated well and the all digital system was suitable to protect an electric power system where over-current protection was needed.

The different manufacturers (AREVA and NxtPhase) provided a current transformer and digital relay that can work together; however, significant mismatch was discovered between the current values measured by the digital relay and by the NxtPhase Optical current transformer when AREVA software was used. The mismatch requires correction from both manufacturers' software.

The details of the findings are as follows:

- The all digital over-current protection system was tested using a realistic high current, which supplied the primary side of the optical CT.
- ASU developed a dedicated test facility that generates high current and high voltage to simulate the current and voltage that occurs in the power network.
- All digital protection system was tested in inverse over-current mode. The system operated well and cleared the faults with proper delay. However, though the relay measured the current dependent time delay accurately, the calculated time delay from the manufacturer's equation was different. This suggests that a software review should be done.
- The test results show that the load current and short duration impulse currents do not produce any tripping signal.
- The DC offset current does not affect the tripping time adversely.
- Because of the lack of equipment, the all digital protection system was not tested in distance protection mode, and the directional over-current relay proper operation was not verified.

6.0 Publications

S. Kucuksari, Y. Ma, G. G. Karady, “Development of Test Facility for Transmission Line Protection,” IEEE Transmission & Distribution Conference, April 2008, Accepted.

7.0 References

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